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Simulation of a Bidirectional DC-DC Boost Converter Using a State-Space Averaged Model

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SIMULATION OF A BIDIRECTIONAL DC-DC BOOST

CONVERTER USING A STATE-SPACE AVERAGED

MODEL

BY

ERIK LANE BENTON

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IN

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UNIVERSITY OF RHODE ISLAND
2017

ABSTRACT

Boost converters are electronic devices that are widely used to power devices that require a higher voltage than the input voltage supply can deliver. When designing boost converter systems, it is difficult to optimize component values without damaging components. Models and simulations of a boost converter are developed to give insight into how to design the system and prevent harm to the boost converter. In particular, a state-space averaged (SSA) model of a DC-DC boost converter that includes a secondary inductor and parasitic resistances is developed. This model is then further developed to match a hardware bidirectional DC-DC boost converter that operates in continuous conduction mode (CCM) and uses voltage-mode with current-mode control. The SSA model is used to simulate an actual hardware boost converter system. The SSA based simulation successfully matched experimental data of the hardware boost converter system at low (10kW) and medium (60 – 120kW) level power outputs, but only approximately matched the system behavior at high (250kW) level power outputs.

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CHAPTER 1

INTRODUCTION

In power electronics, boost converters are widely used to power devices. There are many types of voltage supplies, such as batteries, fuel cells, and generators that can provide a constant voltage. However, the load may require a voltage that is higher than that which can be supplied. The boost converter is responsible for taking this lower input voltage and converting it to the higher voltage required. Boost converters do not generate power; rather, they use an inductor and a switch to store energy and release it at levels greater than that provided by the input [1].

When designing a boost converter, there are many things to consider. High power outputs can require levels of current and voltage that can damage the system [2]. The voltage source or the load may not be ideal and can change in time [3]. There are parasitic resistances in the components that affect the system's ability to deliver the necessary power [4-6]. Secondary components may be required to stabilize the output of the converter [2].

To aid in designing a boost converter, simulations are developed to analyze variables in the system. However, simulations that fully recreate the boost converters can be computationally complex and taxing to run, and due to the non-linear nature of boost converters, provide little insight into how to improve the system. In these cases, averaging techniques that are much less taxing to simulate and can provide the general behavior of the system are used to model the converter [7]. A popular method of

averaging boost converters is the state-space averaging (SSA) method [8-13]. This method averages the models over the possible operating conditions it can exist in, usually regarding time. These averaged models also offer a means to linearize the system using small signal analysis, which aids in developing a control system for the converter [1, 14].

This work will focus on the function of boost converters and how to develop an SSA model that can be implemented as a simulation. First, a background on general, ideal boost converters and how to model those using SSA methods will be presented. Then a complex hardware DC-DC bidirectional boost converter with parasitic resistances, secondary inductor, non-ideal voltage source, and multiple switching devices, will be introduced. An SSA model describing the hardware of the converter will be developed, first describing only its parasitic resistances and secondary inductor. This will then be used to develop a model that includes the non-ideal voltage source and multiple switching devices of the hardware in order to provide a complete description of the converter. This final SSA model will then be implemented as a simulation and a comparison between the model and the hardware will be conducted to determine the accuracy and limitations of the model.

CHAPTER 2

BACKGROUND

2.1 – Boost Converters

      A boost converter is an electronic device that produces a greater output voltage than that of its input voltage without generating power. These devices are widely used in electronic power supplies where the voltage source is not large enough to power the required load. Boost converters store and release energy using an inductor and a switching device to generate the higher voltage. Since these devices do not generate power, there is power lost in the conversion, although this can be minimized by implementing a control system.

2.1.1 – Simple Boost Converter Topology

      The general topology of a simple boost converter can be seen in Fig. 1. There is a constant voltage supply (V_{in}) in series with an inductor (L). This inductor is connected to a diode (D) and a single pole single throw (SPST) switch. The switch connects back to the voltage supply, and the diode connects to a capacitor (C) in parallel with the load, which is modelled as a resistor (R_{load}). This resistor and capacitor then connect back to the negative terminal of the voltage supply.
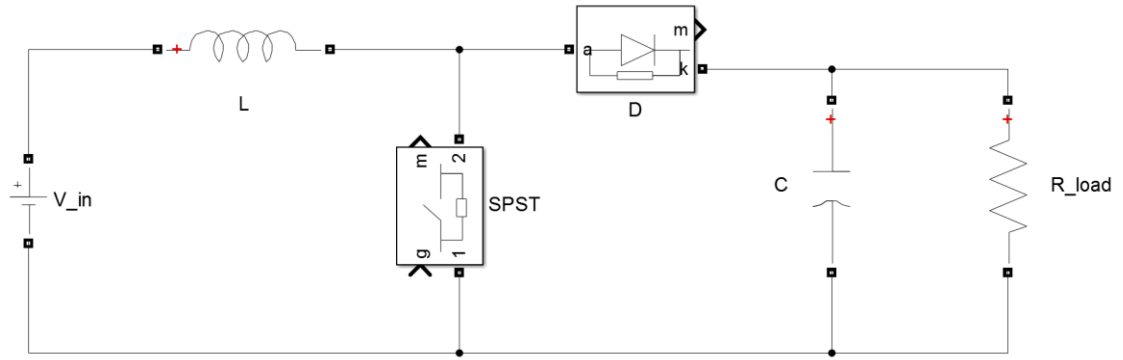
Figure 1 General Topology of a simple boost converter.

2.1.2 – Boost Converter Function

The boost converter converts a low voltage into a higher voltage by using the switch to manipulate the current to store and release energy in the inductor. Inductors are components that resist a change of flow in current. The inductor resists a positive change in the rate of current flowing through it by storing energy in a magnetic field and increasing the voltage across the inductor. When the current through the inductor decreases, the inductor releases this stored energy in an attempt restore the decreasing current, becoming another supply of voltage for the output.

By using the switch, the boost converter causes the current in the inductor to increase and decrease. When the switch is closed, there is little resistance in the circuit from V_{in}, through the inductor and switch, and back to V_{in}. This allows the current output from V_{in} to increase, thus causing the inductor to store energy in its magnetic field. When the switch is opened, there is more resistance in the circuit due to the load. This causes the current through the inductor to drop, therefore causing it to release that

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stored energy. This voltage from the inductor plus that of the input voltage is how the boost converter is able to supply a greater voltage to the load.

During proper operation of the boost converter, the capacitor voltage (v_c) is fully charged to the level of voltage required for the load. Thus, when the switch is closed and the output stage (C and R_{load}) is isolated from the input stage (V_{in} and L), the capacitor acts as the voltage source for the load. This drains the capacitor of its charge, however, when the switch is opened again, the input stage recharges the capacitor. To ensure a near constant output voltage, the capacitor must be chosen so that the RC time constant of the output stage is large enough that the drain on v_c is negligible during the time the switch is open.

The behavior of the boost converter is dependent on how quickly the switch goes through one cycle of open, to close, and back to open. This amount of time is called the switching period (T_s). The switching frequency (f_s) is related to the switching period through the relation

$$f_s = \frac{1}{T_s}$$

The switch can only be in two states, open and closed. The duty ratio is the ratio of time during the switching period that the switch spends in these two operating conditions. The duty ratio for when the switch is open (d_{op}) and for when the switch is closed (d_{cl}) can be found by comparing the amount of time the switch is open (T_{op}) and the amount of time the switch is closed (T_{cl}) to the total switching period.

$$d_{op} = \frac{T_{op}}{T_s}$$

$$d_{cl} = \frac{T_{cl}}{T_s}$$

These ratios have the relationship

$$1 = d_{op} + d_{cl}$$

Due to this relation, it is common to refer to d_{cl} as the duty cycle (d_c) of the system.

Since the boost converter depends so heavily on this switching action, a general calculation of the voltage across the load (V_{load}) can be obtained from the duty cycle and input voltage.

$$V_{load} = \frac{1}{1 - d_c} V_{in}$$

Because of the switching action, the voltage across the load can fluctuate slightly, however it is near constant due to the capacitor C providing voltage for the load when the switch is closed.

2.1.3 – Boost Converter Control

In many applications, the load of the boost converter is not constant, or the voltage supply is not constant [3]. In these cases, the duty cycle of the converter must be controlled to provide a consistent and stable output. There are two popular methods of control for boost converters using closed-loop (or feedback) control: voltage-mode control, and voltage-mode with current-mode control [1, 2, 14]. In these two methods, proportional-integral-derivative (PID) control is used. This work will focus on proportional-integral, or PI, control.

Voltage-Mode Control

In voltage-mode control, the voltage being delivered to the load (V_{load}), is monitored and used to calculate the correct duty cycle for the system. A drop in the

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load voltage from what is required relates to an increase in the duty cycle. A general

block diagram for voltage-mode control can be seen in Fig. 2.
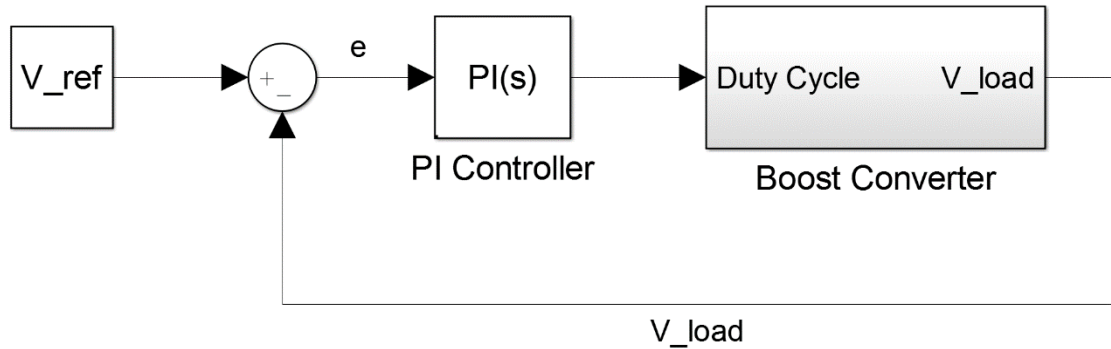
Figure 2 Block diagram of a system utilizing voltage-mode control.

The load voltage is measured and compared to a reference voltage (V_{ref}), and

the difference between these two signals is the error signal (e). This error is sent

through the PI controller which calculates the duty cycle

$$d_c = k_p e + \int (k_i e)dt$$

Where k_p is the proportional gain, and k_i is the integral gain. The gains of the PI

controller are chosen to produce an appropriate duty cycle for the system.

Voltage-Mode with Current-Mode Control

In voltage-mode with current-mode control, both the load voltage and the

current through the inductor are measured to calculate the correct duty cycle for the

system. The current-mode control is used to provide information about the source and

is a form of feedforward control. When used in conjunction with voltage-mode

control, this method can provide better stability for the overall controller. A general

block diagram for this method can be seen in Fig. 3.

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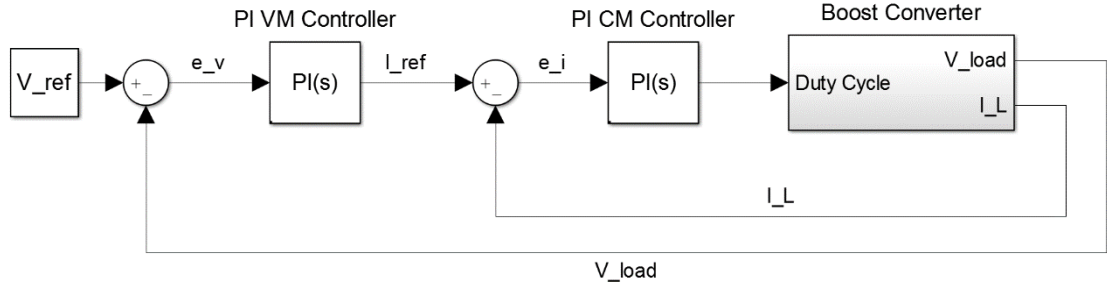
Figure 3 Block diagram of a system utilizing voltage-mode with current-mode control.

Similar to voltage-mode control, the load voltage is measured and compared to a reference, creating an error signal (e_v). However, unlike in pure voltage-mode control, this error is sent through a PI controller to calculate a reference current (I_{ref}). The current through the inductor (I_L) is then compared to this reference current creating another error signal (e_i), which is then used to determine the appropriate duty cycle via a PI controller. Equations for the reference current and duty cycle are shown below

$$I_{ref} = k_{pv}e_v + \int (k_{iv}e_v)dt$$

$$e_i = I_{ref} - I_L$$

$$d_c = k_{pi}e_i + \int (k_{ii}e_i)dt$$

Where k_{pv} and k_{iv} are the proportional gain and integral gain for the voltage-mode controller, and k_{pi} and k_{ii} are the proportional gain and integral gain for the current-mode controller.

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2.1.4 – Boost Converter Conduction Modes

Boost converters have two main modes of conduction. Discontinuous Conduction Mode (*DCM*) and Continuous Conduction Mode (*CCM*) [5-7]. These modes describe the behavior of the current through the inductor. This work will focus on boost converters operating in CCM, but both modes are explored below.

Discontinuous Conduction Mode (DCM)

In DCM, the current through the inductor is not maintained for a period of time during one switching cycle. This means that the current through the inductor remains at 0A for a portion of the switching period when the switch is open. A waveform of the inductor's current can be seen in Fig. 4.
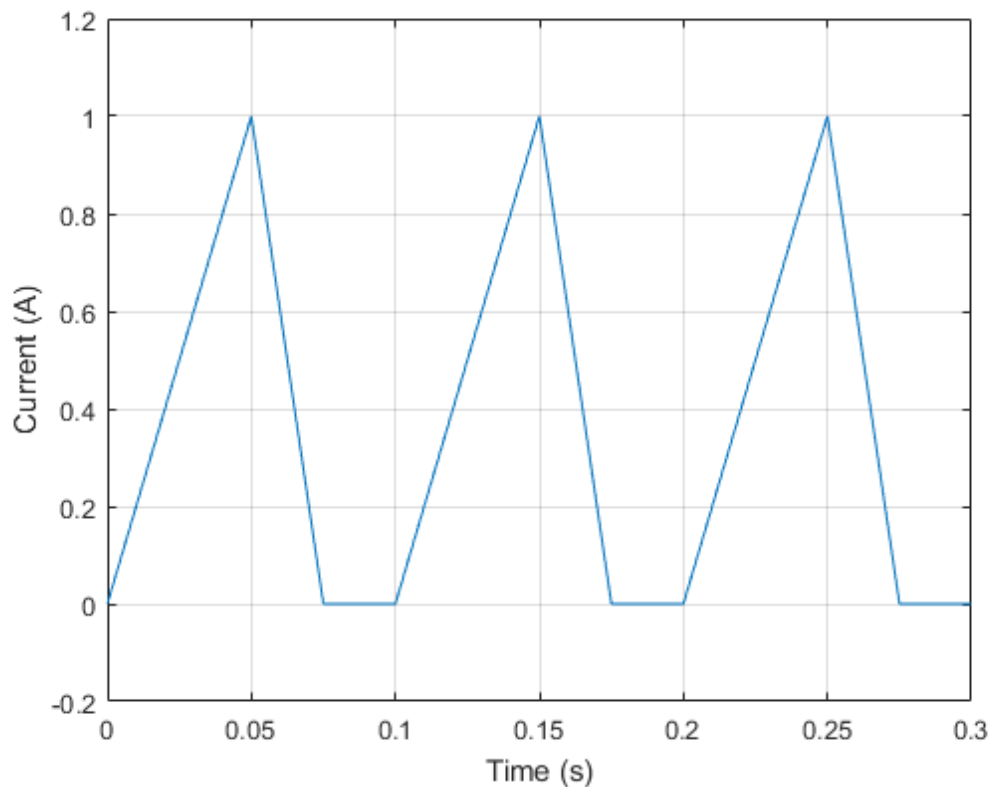
Figure 4 Inductor current for a boost converter operating in DCM.

Continuous Conduction Mode (CCM)

In CCM, the current through the inductor never remains at 0A for a significant portion of time, although it may pass through 0A during a switching period. A waveform of the inductor's current can be seen in Fig. 5.
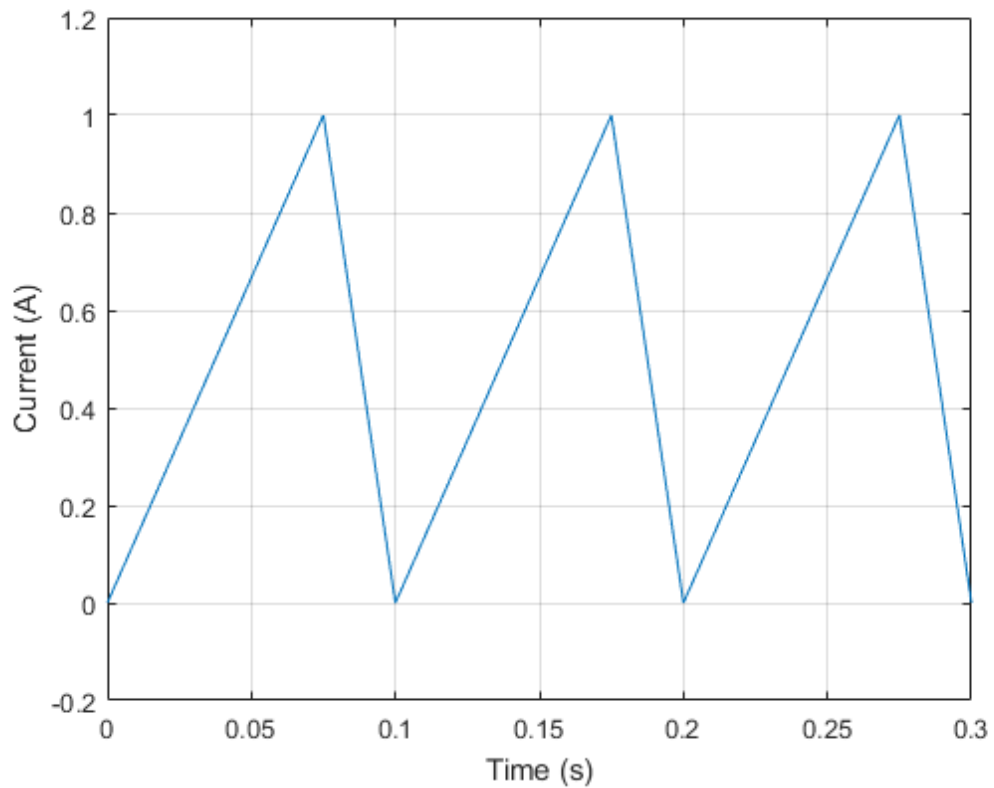
Figure 5 Inductor current for a boost converter operating in CCM.

2.2 – Averaging Techniques

In power electronics, especially that of converters, systems can produce signals that fluctuate rapidly in time [8, 13]. While important in their proper functioning, these fluctuations can make it difficult to explore how the system acts in order to gain an understanding of how to improve their design. To find the general behavior of the system, averaging methods have been developed for these situations. State-space averaging (SSA) is a popular method for averaging a system with signals that undergo small, and rapid changes [1, 7, 8, 13]. SSA defines the different states of a system and averages them with respect to some variable, usually time. A "state" of the system is defined as a permutation of the system for a given operating condition, such as when the switch in a boost converter is open, or closed. SSA offers a way to develop a linearized model of the system using small signal analysis. This allows for the use of control design methods based on linear systems and the Laplace transform [1, 10, 15].

2.2.1 – General Procedure

The general procedure for developing an SSA model of a system involves three main parts. First, the different states, or operating conditions, for the system are defined and the variable for how each state is related is determined. Next, important state-space variables are identified and state-space models for these variables are developed. Finally, these state-space models are averaged together via the averaging variable to find the SSA model. The procedure is shown for an ideal boost converter below.

Definition of the System's States

In an ideal boost converter operating in CCM, there are two states for the

converter. The overall topology and two states can be seen in Fig. 6.
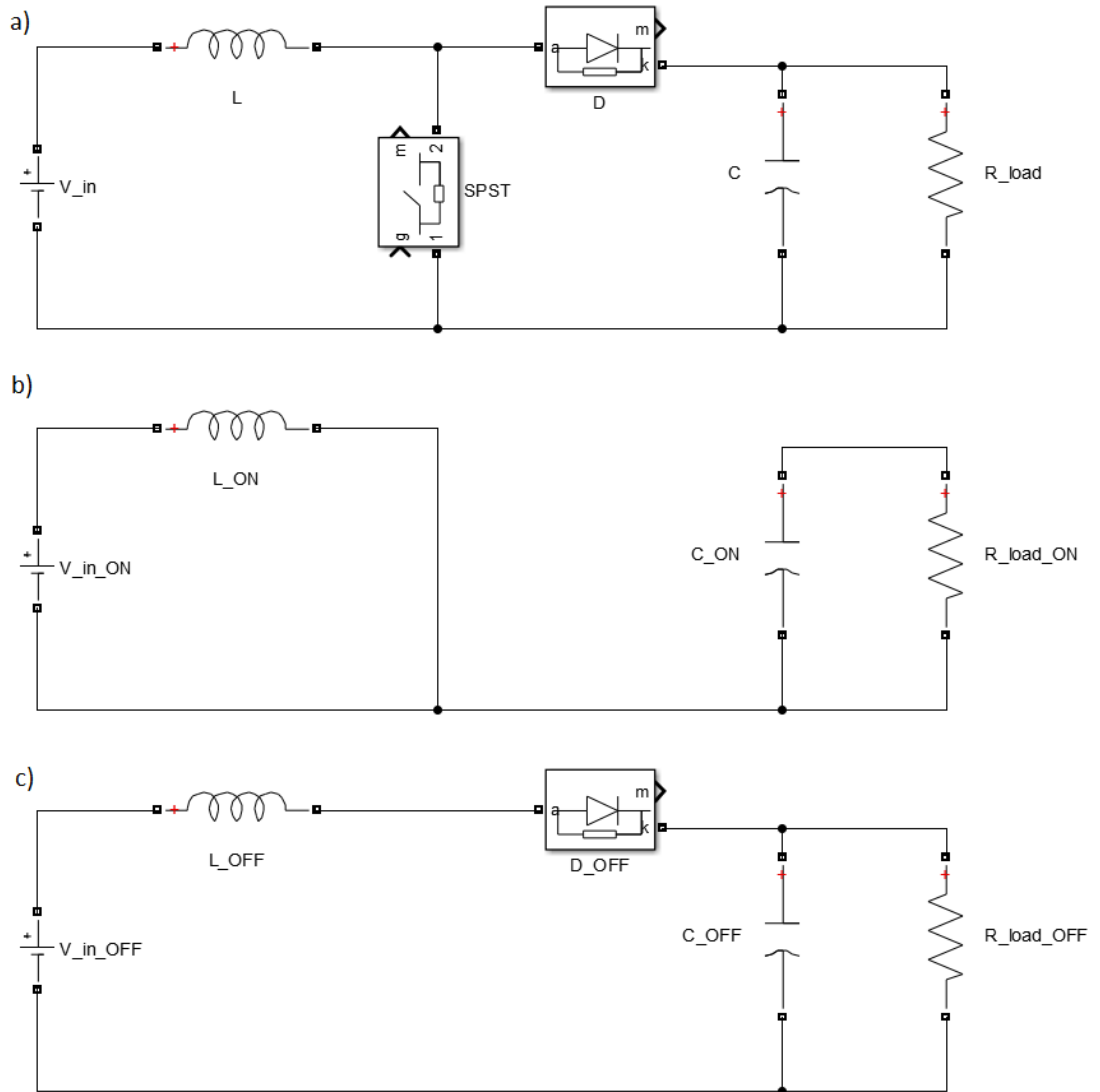
Figure 6 Simple boost converter for SSA (a) Ideal boost converter diagram. (b) "ON"

state of system. (c) "OFF" state of system.

The "ON" state of the converter is defined for when the switch is "ON", or closed. The "OFF" state of the converter is defined for when the switch is "OFF", or open. The constraint that connects these two states is the amount of time that the switch is either in the open or closed position, which is related to the duty cycle of the system.

State Variables and Their Models

In the ideal boost converter, there are two important state variables that define the system. The current through the inductor and the voltage across the capacitor. Using Kirchhoff's Voltage and Current Laws (KVL and KCL respectively), mathematical models for these variables can be found.

In the "ON" state, the switch is closed and current through the inductor (i_L) is only dependent on the voltage source V_{in} and inductor's inductance L. Using KCL, the inductor's current i_L is

$$L\frac{di_L}{dt} = V_{in}$$

Since the switch is closed, the voltage on the capacitor v_c is only dependent on the capacitor's capacitance C and the resistance of the load R_{load}. Using KVL, the capacitor's voltage v_c is

$$C\frac{dv_c}{dt} = -\frac{v_c}{R_{load}}$$

These equations must be written in the state-space form of $\dot{x} = Ax + Bu$, where

$$x = \begin{bmatrix} i_L \\ v_c \end{bmatrix}$$

$$u = [V_{in}]$$

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In the form of $\dot{x} = A_{ON}x + B_{ON}u$, the model for the "ON" state becomes

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{R_{load}C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} [V_{in}]$$

Where

$$A_{ON} = \begin{bmatrix} 0 & 0 \\ 0 & -\dfrac{1}{R_{load}C} \end{bmatrix}$$

$$B_{ON} = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}$$

In the "OFF" state, the switch is open and the current through the inductor now depends on v_c. Using KCL, the inductor's current i_L is

$$L\frac{di_L}{dt} = -v_c + V_{in}$$

Since the switch is open, the capacitor's voltage depends on the current through the inductor. Using KVL, the capacitor's voltage v_c is

$$C\frac{dv_c}{dt} = i_L - \frac{v_c}{R_{load}}$$

In the form of $\dot{x} = A_{OFF}x + B_{OFF}u$, the model for the "OFF" state becomes

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_{load}C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} [V_{in}]$$

Where

$$A_{OFF} = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{R_{load}C} \end{bmatrix}$$

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$$B_{OFF} = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}$$

Averaging the Models

To derive the final SSA model, these two states are averaged over the constraint that relates them, which is the duty cycle of the system. This converter is operating in CCM, thus there are only two duty ratios of a switching period to consider: the ratio for when the system is in the "ON" state (d_{cl}) and when the system is in the "OFF" state (d_{op}). Averaged matrices ($\bar{A}, \bar{B}$) can be written

$$\bar{A} = \left[A_{ON}d_{cl} + A_{OFF}d_{op} \right]$$

$$\bar{B} = \left[B_{ON}d_{cl} + B_{OFF}d_{op} \right]$$

Using the relationship $1 = d_{op} + d_{cl}$ and converting to duty cycle ($d_c = d_{cl}$) these matrices can be rewritten in terms of the duty cycle of the system

$$\bar{A} = [A_{ON}d_c + A_{OFF}(1 - d_c)]$$

$$\bar{B} = [B_{ON}d_c + B_{OFF}(1 - d_c)]$$

The averaged matrices then become

$$\bar{A} = \begin{bmatrix} 0 & -\dfrac{1 - d_c}{L} \\ \dfrac{1 - d_c}{C} & -\dfrac{1}{R_{load}C} \end{bmatrix}$$

$$\bar{B} = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}$$

Putting these in the form $\dot{x} = \bar{A}x + \bar{B}u$ the final SSA model is obtained

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1-d_c}{L} \\ \dfrac{1-d_c}{C} & -\dfrac{1}{R_{load}C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix} [V_{in}]$$

2.2.2 – Application to Controls

Many boost converters rely on control systems to calculate the correct duty cycle to provide the required voltage to the load [9, 10, 13]. As shown in Ch. 2.1.3, the duty cycle is a time varying quantity that depends on the state variables of the system. This means that the control has a multiplicative nonlinearity and sacrifices many of the useful approaches that linear systems offer. To circumvent this, the SSA model is used as a linear approximation to the system and its state equations are used in deriving transfer functions for control analysis. This is the small-signal analysis approach [1, 14, 15].

For small-signal analysis, the state variables and the control parameters are replaced with small perturbed quantities. The previous state equations for the SSA model become

$$L\frac{d(i_L + \tilde{i}_L)}{dt} = -\left(1 - (d_c + \tilde{d}_c)\right)(v_c + \tilde{v}_c) + (V_{in} + \tilde{V}_{in})$$

$$C\frac{d(v_c + \tilde{v}_c)}{dt} = 1 - (d_c + \tilde{d}_c)(i_L + \tilde{i}_L) - \frac{v_c + \tilde{v}_c}{R_{load}}$$

By definition, the non-perturbed quantities are constant in time. These equations become

$$L\frac{d\tilde{i}_L}{dt} = -\left(1 - (d_c + \tilde{d}_c)\right)(v_c + \tilde{v}_c) + (V_{in} + \tilde{V}_{in})$$

$$C\frac{d\tilde{v}_c}{dt} = \left(1 - (d_c + \tilde{d}_c)\right)(i_L + \tilde{i}_L) - \frac{v_c + \tilde{v}_c}{R_{load}}$$

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The system for this model is an ideal boost converter with no losses, therefore there are relations to simplify this expression.

$$V_{in} = (1 - d_c)v_c$$

$$v_c = R_{load}(1 - d_c)i_L$$

And since the perturbations are defined to be small, their products are approximated as zero. Simplifying the above state equations using these relations and approximation, the state equations become

$$L\frac{d\widetilde{i_L}}{dt} = \widetilde{d_c}v_c - (1 - d_c)\widetilde{v_c} + \widetilde{V_{in}}$$

$$C\frac{d\widetilde{v_c}}{dt} = -\widetilde{d_c}i_L + (1 - d_c)\widetilde{i_L} - \frac{\widetilde{v_c}}{R_{load}}$$

The above equations are linear given constant values for the non-perturbed variables and can be used to derive transfer functions for the system. These transfer functions can then be used to find optimal control parameters for the boost converter controller.

CHAPTER 3

HARDWARE CONVERTER

3.1 – Overview

The hardware is a bidirectional DC-DC boost converter that has been

developed to supply power to a hospital during a power outage. This requires the boost

converter to quickly provide stable power over a wide range of outputs. For this, the

converter uses a secondary inductor after the switches, a nonlinear voltage source,

multiple switching devices, and a control system.

3.2 – Requirements for the Hardware

Due to the environment that the hardware is designed for, strict requirements

on its operation have been implemented. The converter must be able to supply the

necessary power output at the desired voltage level in under 50 ms and have the ability

to be recharged many times before requiring replacement components. For these

reasons, large banks of lithium carbide (LiC) supercapacitors are used as the voltage

supply for the hardware. The maximum potential that a bank of these supercapacitors

can maintain is 420V, and the minimum potential is 250V without risking damage.

The converter must also be able to supply a wide range of power outputs, from

10kW to 250kW. The hardware needs to be designed to prevent high levels of current

from damaging components. The converter is designed to have a voltage output of

520V, and the desired power outputs can require currents of greater than 1000A to be necessary.

3.3 – Topology of the Hardware

The converter relies on many devices and systems; the main circuitry for the hardware's boost converter functionality can be seen in Fig. 7.

The supercapacitors can be seen in the top left, feeding directly into the six inductors and switching devices. The currents from the switches then travel to the capacitor and load, then a secondary inductor. The secondary inductor acts to reduce the amount of ripple effect that occurs due to the switching behavior of the boost converter. This is to protect both the load and capacitor from damage.
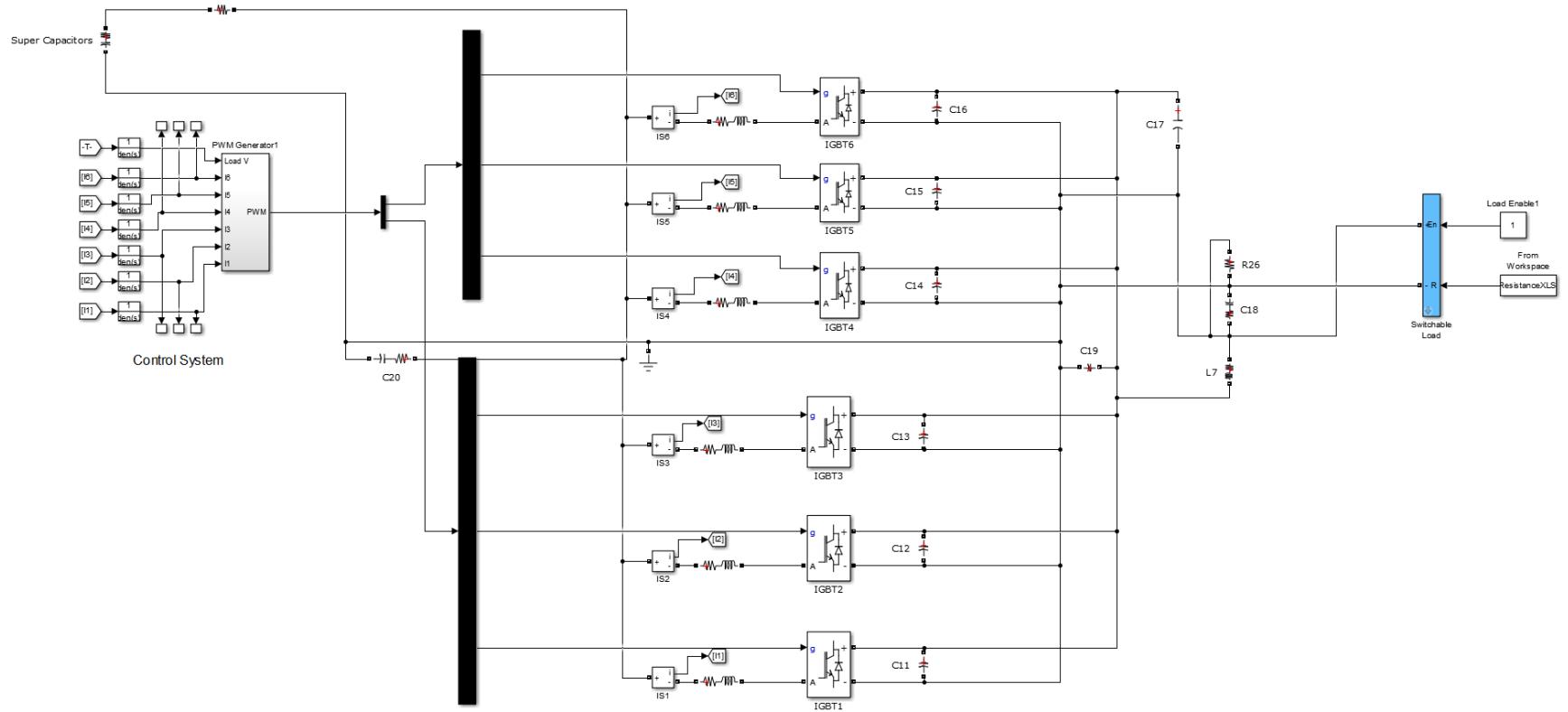
Figure 7 Block diagram of the circuitry for the hardware's boost converter functionality.

3.4 – Non-ideal Voltage Source

The voltage source for the hardware relies on large banks of lithium carbide (LiC) supercapacitors. Each bank contains 108 of these supercapacitors connected in series. For an increase of 60kW in the power output, another bank of supercapacitors is added in parallel with the other banks. For example, for power outputs ranging from 10kW to 50kW, one bank of supercapacitors is connected to the system; for 60kW to 110kW, two banks of supercapacitors are connected. While the system is on, these supercapacitors drop in potential and act as a non-ideal voltage source. In designing models for this system, this drop in potential must be accounted for.

3.5 – Six Inductors and Switching Devices

The hardware for the converter must be able to deliver high levels of current to the load to provide the correct power output. For this, the converter utilizes six inductors and six insulated-gate bipolar transistor (IGBT) switching devices, which distribute the current delivered to the load and prevent damage to the switches. To ensure that the current is distributed evenly, these switches function in a somewhat cascading fashion; for example, in one cycle the switches 1, 2, 3 are open and 4, 5, 6 are closed, in the next cycle switches 2, 3, 4 are open and 5, 6, 1 are closed. However, each switch receives its own duty cycle dependent on the current through its inductor. This means that the cascading nature of the switches is not exact. When the converter first turns on, all the switches are initialized with the same duty cycle and they cascade perfectly, but when the duty cycles begin to differ, they cycle independently of each other.

3.6 – Hardware Control System

The voltage source and load of the converter are non-ideal and can change in time. To ensure the proper output of the converter, a control system is implemented to regulate the switching action of the IGBTs. A voltage-mode with current-mode controller is used for each switch. There is one voltage-mode PI controller that works in series with six current-mode PI controllers in the system. A general block diagram of the system can be seen in Fig. 8.
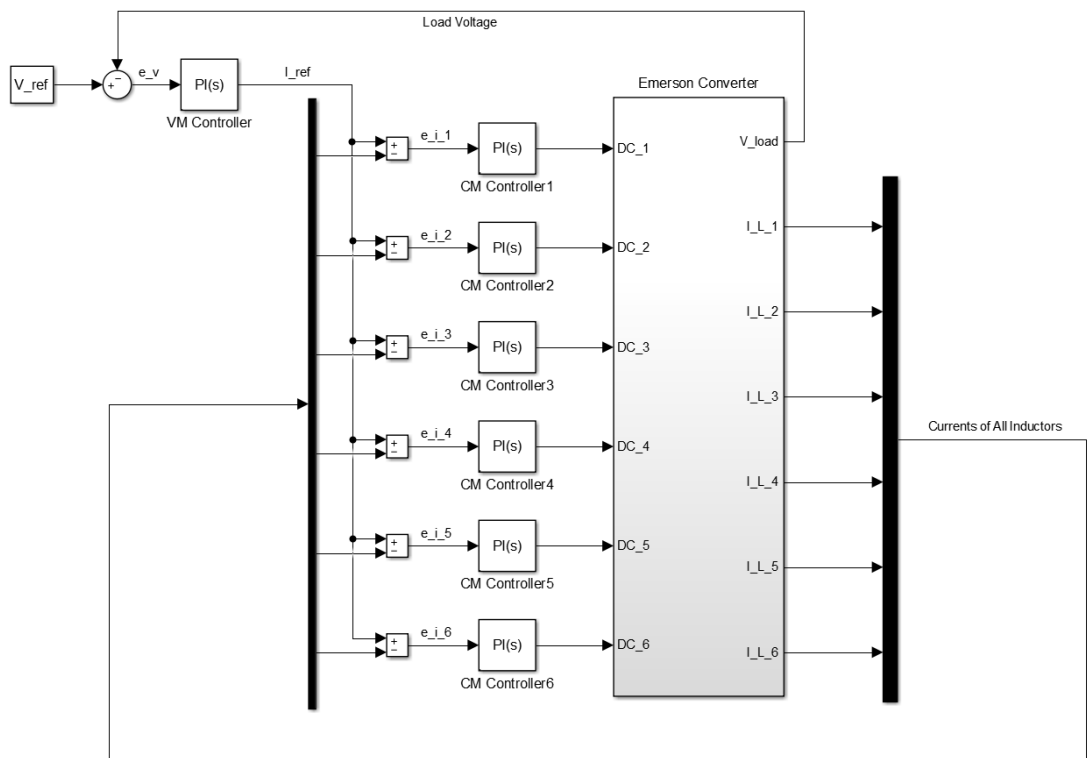
Figure 8 Block diagram of the control system for the hardware converter.

The capacitor voltage is measured and compared to the reference voltage. The difference between these signals is then sent through a PI controller which calculates an appropriate current for the system, named the *commanded current*. The current through each inductor and IGBT is measured and compared to this commanded current. The difference between the signals is then sent through a PI controller for each IGBT and the appropriate duty cycle for that IGBT is calculated.

CHAPTER 4

DEVELOPING AN SSA MODEL OF THE HARDWARE

4.1 – Overview

The state-space average model of the hardware was developed in an iterative process. First, a model based on a general, ideal boost converter was designed (see Ch. 2.2.1). This general model was then used to develop a model of the converter's hardware that accounts for the secondary inductor and parasitic resistances in the system. The second model was then used to create a model including the non-ideal nature of the supercapacitor voltage source. Finally, the non-ideal voltage source model was used to derive a final SSA model that accounts for the six inductors and switching device pairs, and six independent duty cycles in the hardware. The final SSA model has eight state variables with no system input.

4.2 – Secondary Inductor and Parasitic Resistances SSA Model

The SSA model of the general, ideal boost converter developed in Ch. 2.2.1 was further developed to include the secondary inductor and parasitic resistances found in the hardware of the converter that operates in CCM. The secondary inductor acts to reduce the amount of ripple in the current that is delivered to the load. This directly affects the power output of the converter and thus the required voltage from the voltage source and the capacitor that is in parallel with the load.

Parasitic resistances in the system play an important role in the converter's ability to provide the required voltage for the load due to the nature of how a boost converter functions [4-6]. Since the hardware uses real-world components, the capacitors, switches, and inductors all have non-negligible resistances. This second model accounts for these parasitic resistances.

4.2.1 –Topology and States of Second Model

The overall topology and the possible states for the second model can be seen in Fig. 9. Note that in Fig. 9 (b) & (c), the resistances of inductor L_1 (R_{L1}) and the resistances for the voltage source and its connections have been summed and are represented by a single resistance before the switch (R_{BS}).
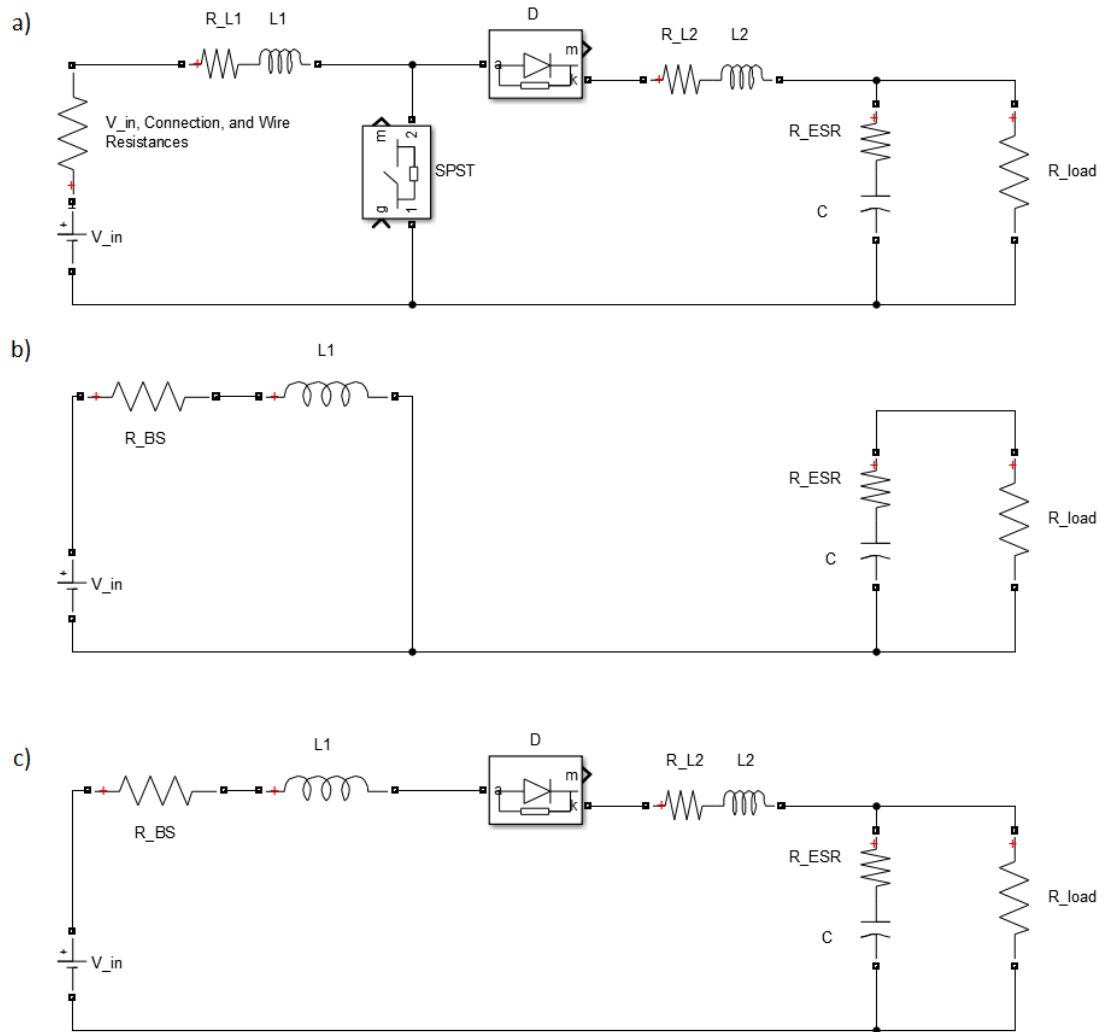
Figure 9 Second model of boost converter for SSA (a) Overall topology for Second model (b) "ON" state for the system (c) "OFF" state for the system.

Similar to the ideal boost converter, the "ON" state of the converter is defined for when the switch is "ON", or closed, and the "OFF" state of the converter is defined for when the switch is "OFF", or open. Once again, the constraint that connects these two states is the amount of time that the switch is either open or closed, which is related to the duty cycle of the system

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4.2.2 – Define State-Variables and Their Models

The key state variables in this model are the current through L_1 (i_L) and the voltage across the capacitor (v_c). Using Kirchhoff's Voltage and Current Laws (KVL and KCL, respectively), equations for these state variables can be found.

In the "ON" state the switch is closed and the current that passes through the first inductor is dependent on the input voltage (V_{in}) and the voltage drop for the resistance before the switch (R_{BS}). Using KCL, the current is

$$L_1 \frac{di_L}{dt} = -R_{BS}i_L + V_{in}$$

During the "ON" state, the voltage of the capacitor is only dependent on the capacitor's equivalent series resistance (R_{ESR}) and the resistance of the load R_{load}. Using KVL, the voltage across the capacitor is

$$C \frac{dv_c}{dt} = -\frac{v_c}{R_{load} + R_{ESR}}$$

These equations must be written in the state-space form of $\dot{x} = Ax + Bu$, where

$$x = \begin{bmatrix} i_L \\ v_c \end{bmatrix}$$

$$u = [V_{in}]$$

In the form of $\dot{x} = A_{ON}x + B_{ON}u$, the model for the "ON" state becomes

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = \begin{bmatrix} -\frac{R_{BS}}{L_1} & 0 \\ 0 & -\frac{1}{(R_{load} + R_{ESR})C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \end{bmatrix} [V_{in}]$$

Where

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$$A_{ON} = \begin{bmatrix} -\dfrac{R_{BS}}{L_1} & 0 \\ 0 & -\dfrac{1}{(R_{load} + R_{ESR})C} \end{bmatrix}$$

$$B_{ON} = \begin{bmatrix} \dfrac{1}{L_1} \\ 0 \end{bmatrix}$$

In the "OFF" state, the switch is open and the current through the inductor is now affected by the capacitor and the secondary inductor. Using KCL, the current through the inductor is

$$(L_1 + L_2)\frac{di_L}{dt} = -(R_{BS} + R_{L2})i_L - v_c + V_{in}$$

While in the "OFF" state, the voltage across the capacitor is affected by its own voltage and the current through L_1. Using KVL, the voltage across the capacitor is

$$C\frac{dv_c}{dt} = \frac{R_{load}}{R_{load} + R_{ESR} + R_7}i_L - \frac{v_c}{R_{load} + R_{ESR}}$$

In the form of $\dot{x} = A_{OFF}x + B_{OFF}u$, the model for the "OFF" state becomes

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = \begin{bmatrix} -\dfrac{(R_{BS} + R_{L2})}{(L_1 + L_2)} & -\dfrac{1}{(L_1 + L_2)} \\ \dfrac{R_{load}}{(R_{load} + R_{ESR} + R_7)C} & -\dfrac{1}{(R_{load} + R_{ESR})C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{(L_1 + L_2)} \\ 0 \end{bmatrix} [V_{in}]$$

Where

$$A_{OFF} = \begin{bmatrix} -\dfrac{(R_{BS} + R_{L2})}{(L_1 + L_2)} & -\dfrac{1}{(L_1 + L_2)} \\ \dfrac{R_{load}}{(R_{load} + R_{ESR} + R_7)C} & -\dfrac{1}{(R_{load} + R_{ESR})C} \end{bmatrix}$$

$$B_{OFF} = \begin{bmatrix} \dfrac{1}{(L_1 + L_2)} \\ 0 \end{bmatrix}$$

4.2.3 – Averaging the States of the Second SSA Model

To derive the SSA model, these two states are averaged over the duty cycle of the system. This converter is operating in CCM, thus there are only two segments of time during one switching period to consider for averaging; during $d_c T_s$ (the "ON" state), and during $(1 - d_c)T_s$ (the "OFF" state). The averaged matrices $(\bar{A}, \bar{B})$ can be written

$$\bar{A} = [A_{ON}d_c + A_{OFF}(1 - d_c)]$$

$$\bar{B} = [B_{ON}d_c + B_{OFF}(1 - d_c)]$$

The averaged matrices become

$$\bar{A} = \begin{bmatrix} -\dfrac{R_{BS}}{L_1}d_c - \dfrac{(R_{BS} + R_{L2})}{(L_1 + L_2)}(1 - d_c) & -\dfrac{1 - d_c}{(L_1 + L_2)} \\ \dfrac{R_{load}}{(R_{load} + R_{ESR} + R_7)C}(1 - d_c) & -\dfrac{1}{(R_{load} + R_{ESR})C} \end{bmatrix}$$

$$\bar{B} = \begin{bmatrix} \dfrac{d_c}{L_1} + \dfrac{(1 - d_c)}{(L_1 + L_2)} \\ 0 \end{bmatrix}$$

Putting these in the form $\dot{x} = \bar{A}x + \bar{B}u$ the SSA model is obtained

$$\begin{bmatrix} \dot{i_L} \\ \dot{v_c} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_{BS}}{L_1}d_c - \dfrac{(R_{BS} + R_{L2})}{(L_1 + L_2)}(1 - d_c) & -\dfrac{1 - d_c}{(L_1 + L_2)} \\ \dfrac{R_{load}}{(R_{load} + R_{ESR} + R_7)C}(1 - d_c) & -\dfrac{1}{(R_{load} + R_{ESR})C} \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix}$$

$$+ \begin{bmatrix} \dfrac{d_c}{L_1} + \dfrac{(1 - d_c)}{(L_1 + L_2)} \\ 0 \end{bmatrix} [V_{in}]$$

4.3 – Final SSA Model

The voltage source in the hardware for the converter is non-ideal as the voltage in the supercapacitors drops in time proportional to the current required by the load.

To compensate for this, the SSA model that has been developed is of a higher-order than the previous model, with the supercapacitor voltage as a state variable instead of as an input for the system.

The hardware utilizes six switching devices and inductors, and the current through each must be monitored. This requires that the developed SSA model must measure these currents, therefore each inductor's current is a state variable. The switches also receive their own duty cycle independently of each other. This means that there can be many states for the system. However, this will be simplified during the initial development of this model and expanded upon after a simpler model has first been defined.

4.3.1 – Topology and States of the Final SSA Model

In this initial model of the hardware, the six switching devices and their inductors have been simplified to a single switch and inductor. Since the converter operates in CCM, there are only two states for the system. A diagram of this simplified converter and its states is shown in Fig. 10. Note that the six switching devices and their inductors will be represented after the development of this model.
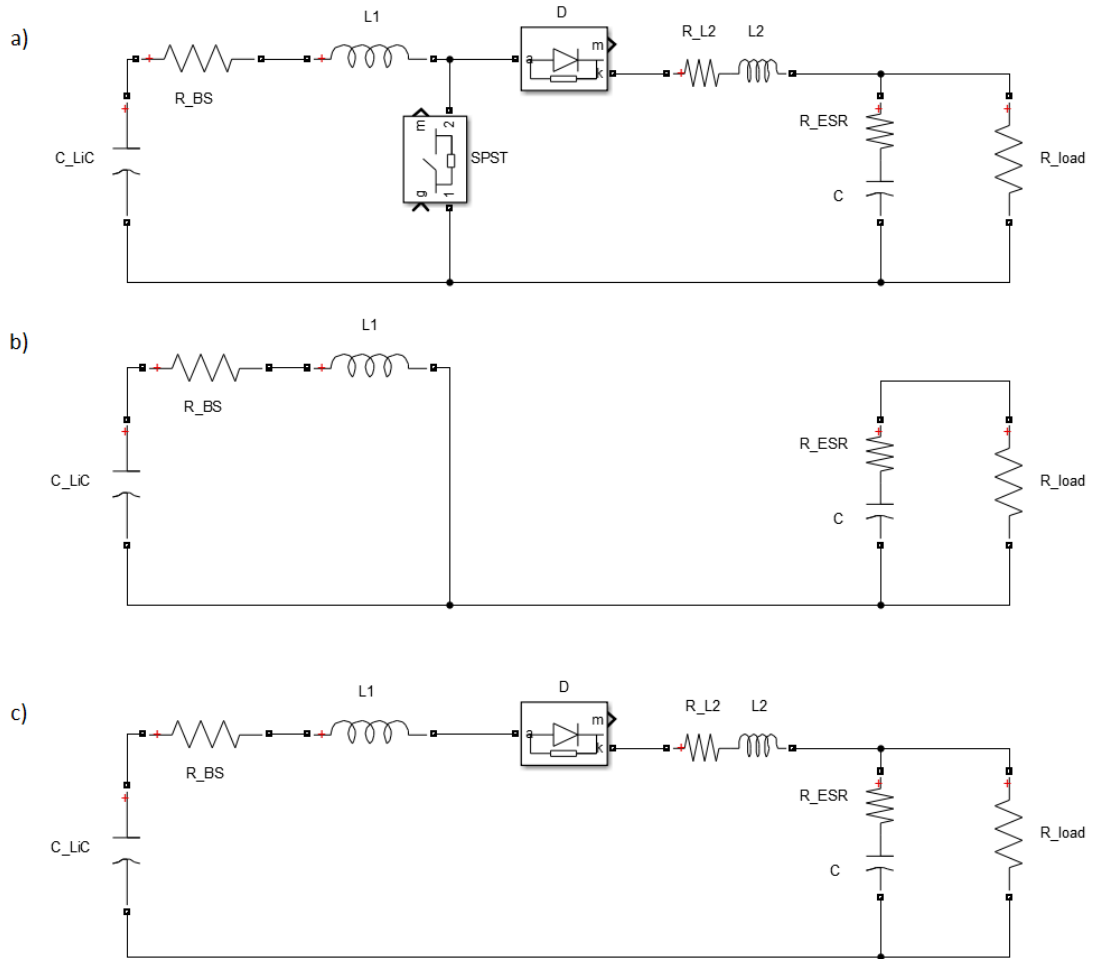
Figure 10 Final SSA model (a) Overall topology for Final SSA model (b) "ON" state for the system (c) "OFF" state for the system.

The state of the switch defines the two states of the converter. The "ON" state corresponds to when the switch is closed, and the "OFF" state corresponds to when the switch is open. The duty cycle is the constraint over which the two states will be averaged.

4.3.2 - Define State-Variables and Their Models

Important key variables for the system are the current through the inductor (i_L), the voltage across the capacitor in parallel with the load (v_c), and the voltage supplied by the banks of supercapacitors (v_{LiC}).

In the "ON" state the switch is closed and the current that passes through the inductor is dependent on the inductance of the inductor, the voltage drop from the resistance before the switch, and the voltage supplied by the supercapacitors. Using KCL, the current for the inductor i_L is

$$L_1 \frac{di_L}{dt} = -R_{BS} i_L + v_{LiC}$$

During the "ON" state the voltage of the capacitor does not interact with the inductor or voltage supply, and is only dependent on the capacitor's internal resistance (R_{ESR}) and the resistance of the load R_{load}. Using KVL, the voltage across the capacitor v_c is

$$C \frac{dv_c}{dt} = -\frac{v_c}{R_{load} + R_{ESR}}$$

The voltage for the supercapacitors in the "ON" state is dependent on the current through the inductor and the capacitance of all the supercapacitors in the bank. Using KVL, the voltage for the voltage supply v_{LiC} is

$$C_{LiC} \frac{dv_{LiC}}{dt} = -i_L$$

These equations must be written in the state-space form of $\dot{x} = Ax + Bu$, where

$$x = \begin{bmatrix} i_L \\ v_c \\ v_{LiC} \end{bmatrix}$$

Note that there is no longer an input for the system since the voltage source is now a state variable.

In the form of $\dot{x} = A_{ON}x + B_{ON}u$, these equations become

$$\begin{bmatrix} \dot{\iota}_L \\ \dot{v}_c \\ \dot{v}_{LiC} \end{bmatrix} = \begin{bmatrix} -\dfrac{R_{BS}}{L_1} & 0 & \dfrac{1}{L_1} \\ 0 & -\dfrac{1}{(R_{load} + R_{ESR})C} & 0 \\ -\dfrac{1}{C_{LiC}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_c \\ v_{LiC} \end{bmatrix}$$

Where the A_{ON} matrix takes the form of

$$A_{ON} = \begin{bmatrix} -\dfrac{R_{BS}}{L_1} & 0 & \dfrac{1}{L_1} \\ 0 & -\dfrac{1}{(R_{load} + R_{ESR})C} & 0 \\ -\dfrac{1}{C_{LiC}} & 0 & 0 \end{bmatrix}$$

In the "OFF" state the switch is closed and the inductor interacts with the entirety of the system. Using KCL, the equation for the inductor's current i_L is

$$(L_1 + L_2)\frac{di_L}{dt} = -(R_{BS} + R_{L2})i_L - v_c + v_{LiC}$$

Using KVL, the equation for the voltage across the load capacitor during the "OFF" state v_c is

$$C\frac{dv_c}{dt} = \frac{R_{load}}{R_{load} + R_{ESR} + R_7}i_L - \frac{v_c}{R_{load} + R_{ESR}}$$

The voltage in across the supercapacitors in the "OFF" state remains dependent on only the current through the inductor, similar to during the "ON" state. Using KVL, the voltage for the voltage supply v_{LiC} is

$$C_{LiC}\frac{dv_{LiC}}{dt} = -i_L$$

In the form of $\dot{x} = A_{OFF}x + B_{OFF}u$, these equations become

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$$\begin{bmatrix} \dot{\iota}_L \\ \dot{v}_c \\ \dot{v}_{LiC} \end{bmatrix} = \begin{bmatrix} -\dfrac{(R_{BS} + R_{L2})}{(L_1 + L_2)} & -\dfrac{1}{(L_1 + L_2)} & \dfrac{1}{(L_1 + L_2)} \\ \dfrac{R_{load}}{(R_{load} + R_{ESR} + R_7)C} & -\dfrac{1}{(R_{load} + R_{ESR})C} & 0 \\ -\dfrac{1}{C_{LiC}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_L \\ v_c \\ v_{LiC} \end{bmatrix}$$

Where the A_{OFF} matrix takes the form of

$$A_{OFF} = \begin{bmatrix} -\dfrac{(R_{BS} + R_{L2})}{(L_1 + L_2)} & -\dfrac{1}{(L_1 + L_2)} & \dfrac{1}{(L_1 + L_2)} \\ \dfrac{R_{load}}{(R_{load} + R_{ESR} + R_7)C} & -\dfrac{1}{(R_{load} + R_{ESR})C} & 0 \\ -\dfrac{1}{C_{LiC}} & 0 & 0 \end{bmatrix}$$

4.3.3 – Averaging the States of the Final SSA Model

To derive the final SSA model of the simplified hardware converter, the two states are averaged over the duty cycle of the system. The two segments of time during one switching period to consider for averaging are: during $d_c T_s$ (the "ON" state), and during $(1 - d_c)T_s$ (the "OFF" state). The averaged matrices $(\bar{A}, \bar{B})$ can be written

$$\bar{A} = [A_{ON}d_c + A_{OFF}(1 - d_c)]$$

$$\bar{B} = [B_{ON}d_c + B_{OFF}(1 - d_c)]$$

The SSA model for the simplified system becomes

$$
\begin{bmatrix} \dot{\iota_L} \\ \dot{v_c} \\ \dot{v}_{LiC} \end{bmatrix}
$$

$$
= \begin{bmatrix}
-\dfrac{R_{BS}}{L_1}d_c - \dfrac{(R_{BS} + R_{L2})}{(L_1 + L_2)}(1 - d_c) & -\dfrac{1 - d_c}{(L_1 + L_2)} & \dfrac{d_c}{L_1} + \dfrac{(1 - d_c)}{L_1 + L_2} \\
\dfrac{R_{load}}{(R_{load} + R_{ESR} + R_7)C}(1 - d_c) & -\dfrac{1}{(R_{load} + R_{ESR})C} & 0 \\
-\dfrac{1}{C_{LiC}} & 0 & 0
\end{bmatrix}
\begin{bmatrix} i_L \\ v_c \\ v_{LiC} \end{bmatrix}
$$

4.3.4 – SSA Model Accounting for Six Inductors, Switches, and Duty Cycles

Due to the fact that each switch receives its own duty cycle independently of the other switches, there are a total of 2^6, or 64, possible states that the system could exist in at any given time. This requires a very complex SSA averaged model dependent on future knowledge of the duty cycle for each switch at every moment in time. To simplify the model, a compromise was made in designing a model that incorporates all six inductors and switches. Rather than predetermining how each switch will function in regards to every other switch at every moment in time, the concept of the developed model is an overlay of six of the previous models, each with their own duty cycle. A diagram for the system is shown in Fig. 11.
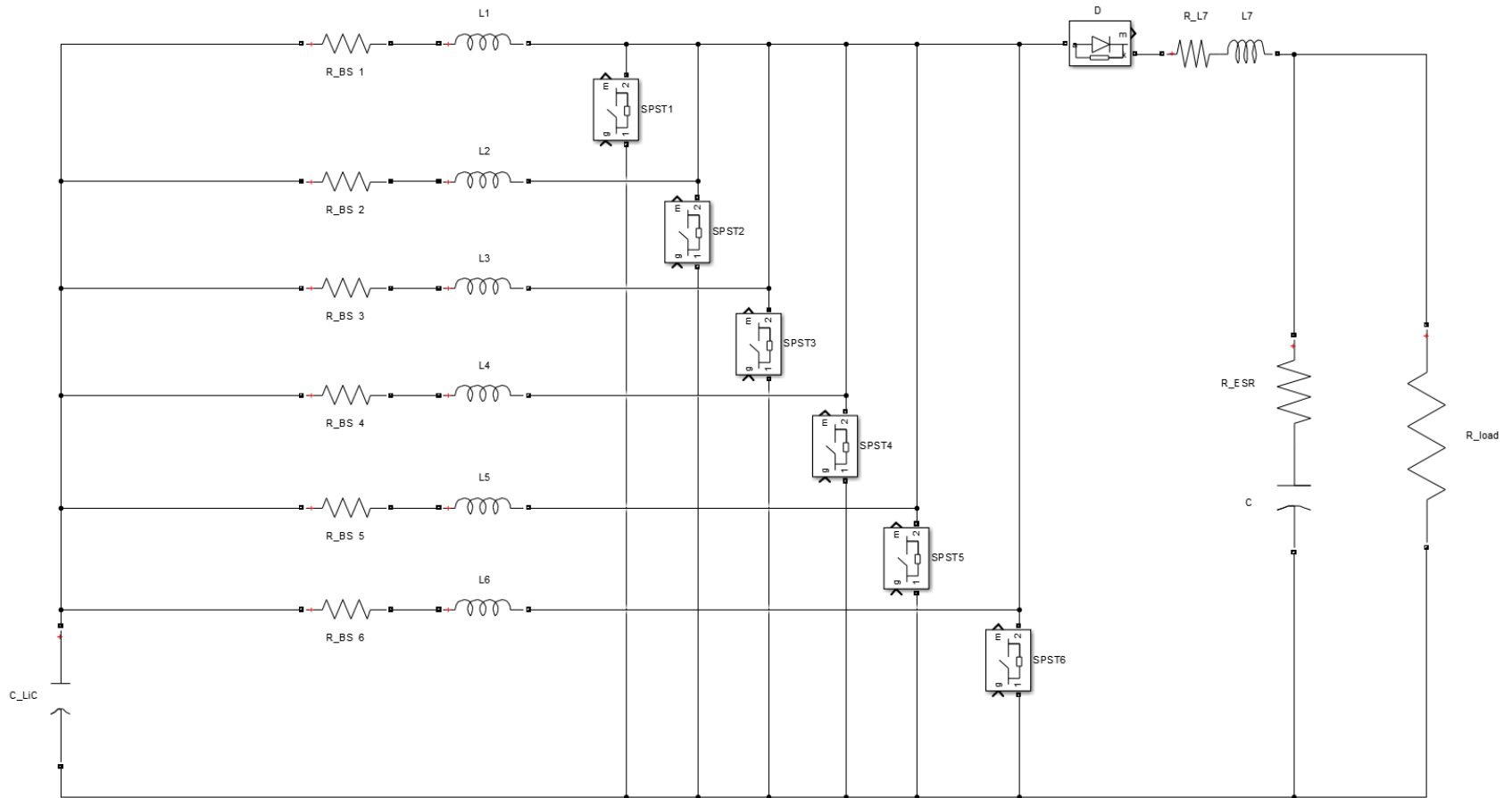
Figure 11 Diagram of the topology for the hardware converter including all six inductors and switches.

By utilizing the previous model and expanding upon it to include all six

inductor currents and duty cycles, the final SSA model for the hardware is obtained.

$$
\begin{bmatrix} \dot{\iota}_{L1} \\ \dot{\iota}_{L2} \\ \dot{\iota}_{L3} \\ \dot{\iota}_{L4} \\ \dot{\iota}_{L5} \\ \dot{\iota}_{L6} \\ \dot{v}_C \\ \dot{v}_{LiC} \end{bmatrix} = \begin{bmatrix} a_1 & 0 & 0 & 0 & 0 & 0 & c_1 & d_1 \\ 0 & a_2 & 0 & 0 & 0 & 0 & c_2 & d_2 \\ 0 & 0 & a_3 & 0 & 0 & 0 & c_3 & d_3 \\ 0 & 0 & 0 & a_4 & 0 & 0 & c_4 & d_4 \\ 0 & 0 & 0 & 0 & a_5 & 0 & c_5 & d_5 \\ 0 & 0 & 0 & 0 & 0 & a_6 & c_6 & d_6 \\ b_1 & b_2 & b_3 & b_4 & b_5 & b_6 & p & 0 \\ q & q & q & q & q & q & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ i_{L5} \\ i_{L6} \\ v_C \\ v_{LiC} \end{bmatrix}
$$

Where

$$
a_i = -\frac{R_{BSi}}{L_i} d_{ci} - \frac{(R_{BSi} + R_{L7})}{(L_i + L_7)}(1 - d_{ci})
$$

$$
b_i = \frac{R_{load}}{(R_{load} + R_{ESR} + R_7)C}(1 - d_{ci})
$$

$$
c_i = -\frac{1 - d_{ci}}{(L_i + L_2)}
$$

$$
d_i = \frac{d_{ci}}{L_i} + \frac{(1 - d_{ci})}{L_i + L_7}
$$

$$
q = -\frac{1}{C_{LiC}}
$$

$$
p = -\frac{1}{(R_{load} + R_{ESR})C}
$$

CHAPTER 5

COMPARISON OF SIMULATION AND HARDWARE

6.1 – Overview

The SSA model of the hardware was implemented in Matlab/Simulink as a

simulation (see A.1 for an overview of the simulation). Due to the requirement for a

wide range of power outputs, the hardware's SSA model simulation was compared to

the performance of the hardware at 10kW, 60kW, 120kW, and 250kW. Each of these

power levels required the addition of another bank of supercapacitors for the voltage

source. Important variables that were compared include: the load power, current, and

voltage, the voltage level of the supercapacitors, the current through each inductor,

and each duty cycle.

6.2 – Simulation Procedure

The hardware converter was tested for a given power output and measurements

of important signals were monitored and recorded. These measurements were taken

using current and voltage sensors that recorded the data through a filter. Due to this,

the recorded data is sampled and the current through the inductors appears to have no

ripple effect.

Values necessary for the simulation, such as the initial voltage of the

supercapacitors, the initial duty cycle values, and the gains for the controllers were

input into the Matlab/Simulink simulation. Of key importance was the resistance of

the load, which changed in time due to its implementation in the hardware. The load

resistance was calculated using the recorded data for the current and voltage of the

load through the relation

$$R_{load} = \frac{V_{load}}{I_{load}}$$

The resistance as a function of time was then fed directly into the simulation

while it ran. The simulation was then performed and the important signals were

recorded and saved. A comparison of the real-world data and the simulation data were

plotted and compared. Note that only two inductor currents (i_{L3} and i_{L6}) and the duty

cycle for their respective switches (d_{c3} and d_{c6}) are plotted due to the high level of

similarity between all inductors and switches.

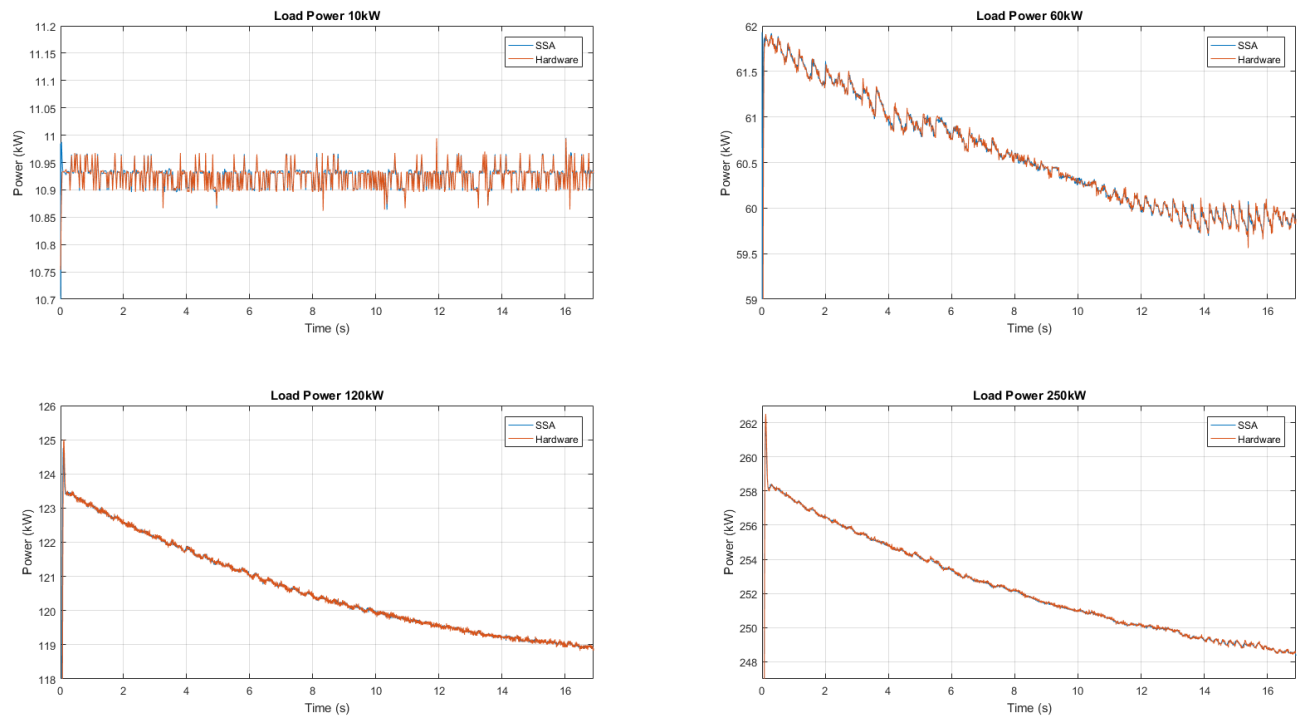## 5.3 – Simulation and Hardware Comparison Results

5.3.1 – Load Power

Figure 12 Power delivered to the load for each trial. (Blue) Results for the SSA model simulation. (Orange) Results for the hardware.
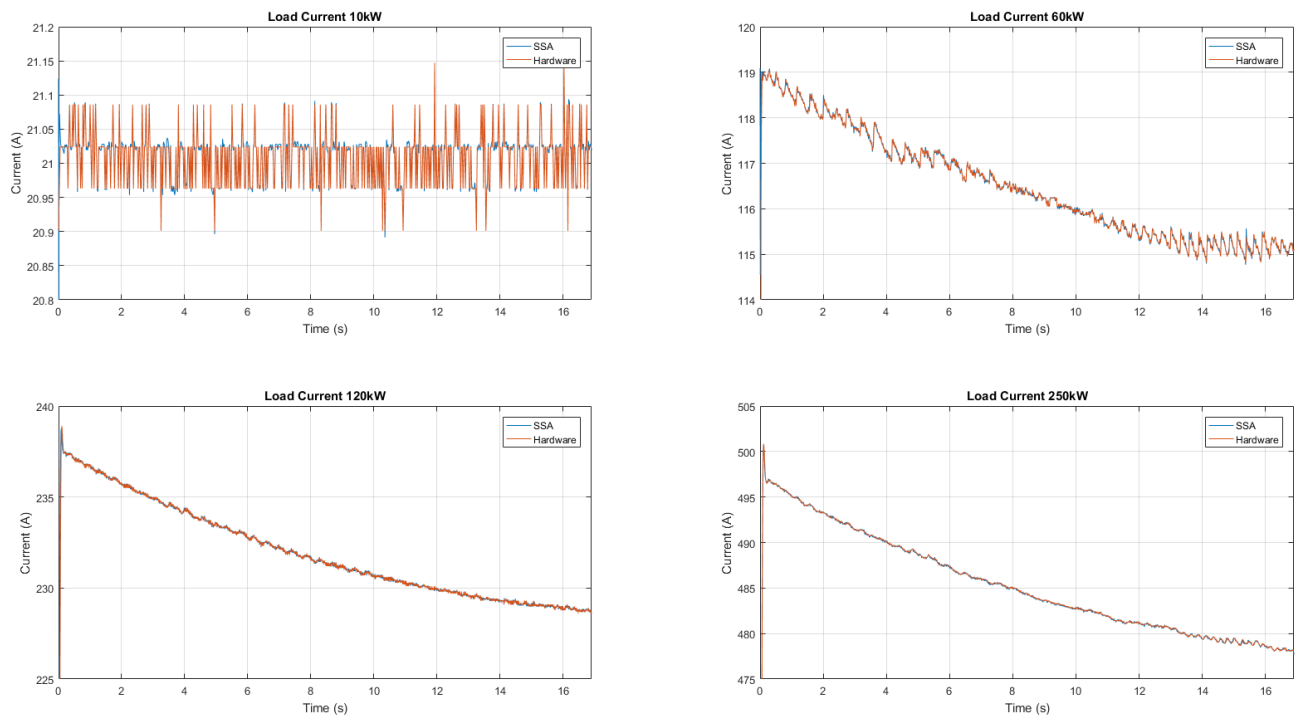
5.3.2 – Load Current

Figure 13 Current delivered to the load for each trial. (Blue) Results for the SSA model simulation. (Orange) Results for the hardware.

5.3.3 – Load Voltage
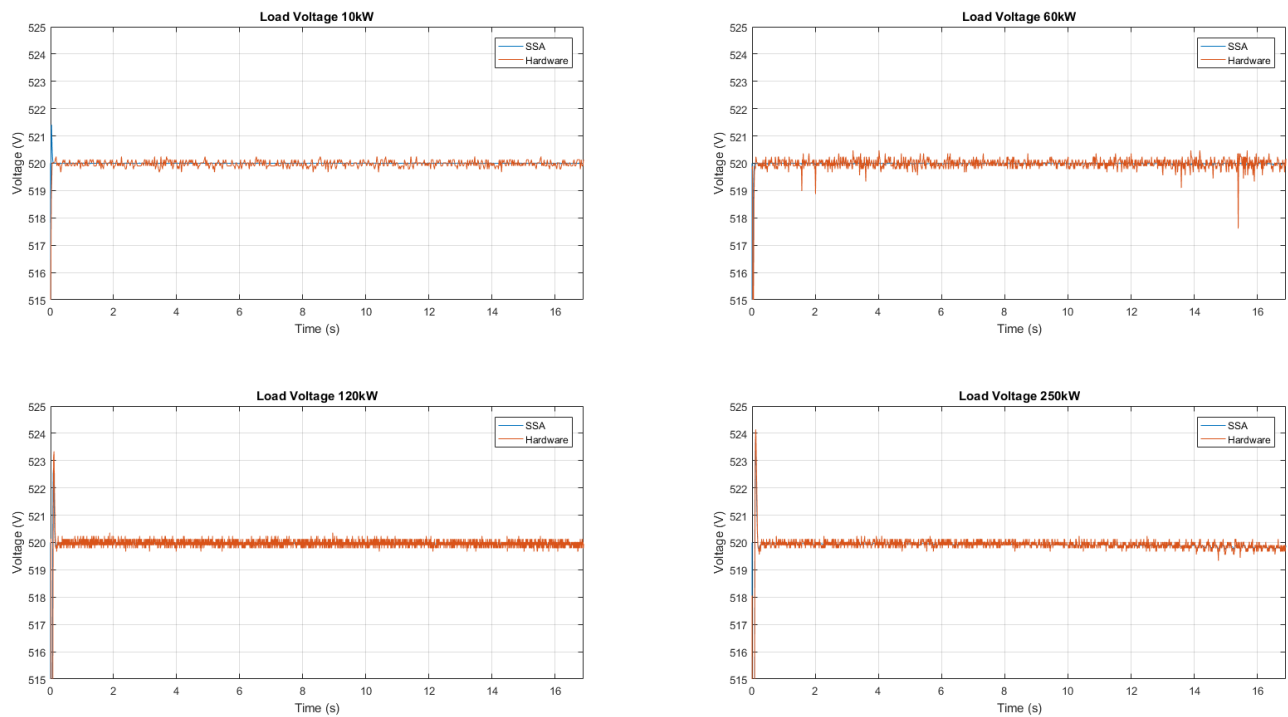
Figure 14 Voltage delivered to the load for each trial. (Blue) Results for the SSA model simulation. (Orange) Results for the hardware.

5.3.4 – Super Capacitor Voltage
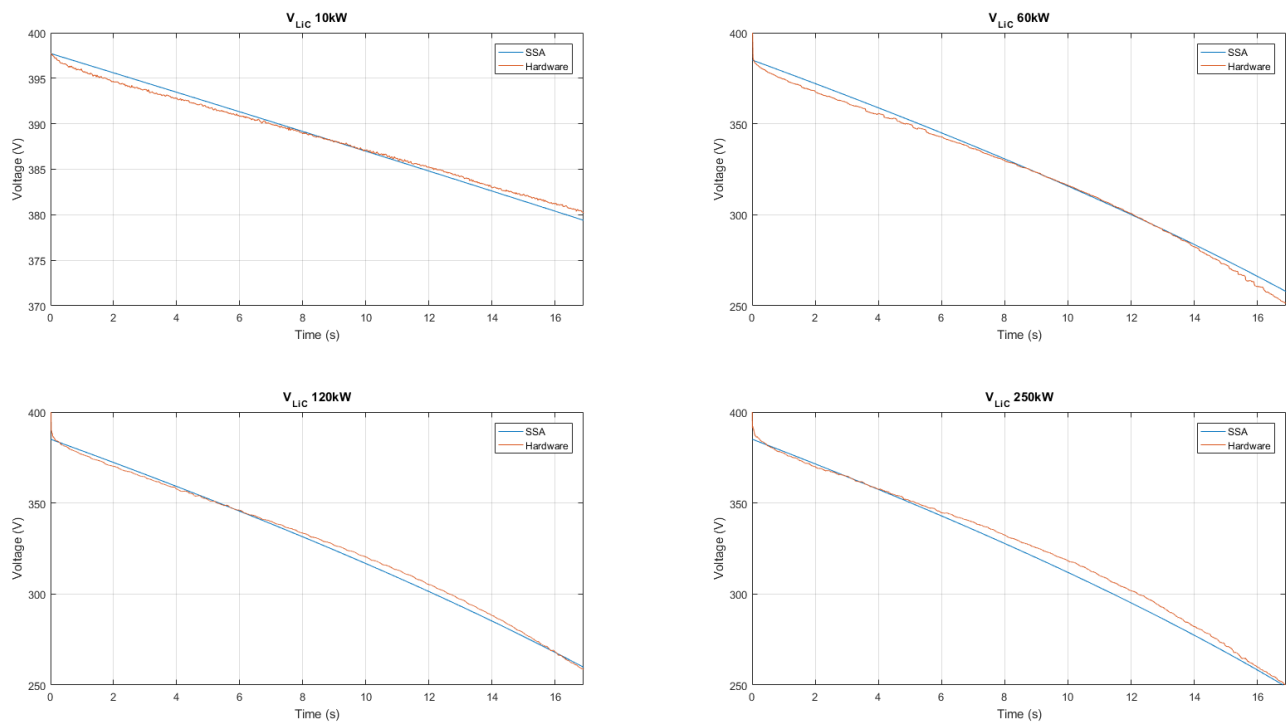
Figure 15 Voltage of the banks of supercapacitors for each trial. (Blue) Results for the SSA model simulation. (Orange) Results for the hardware.

5.3.5 – Inductor Currents
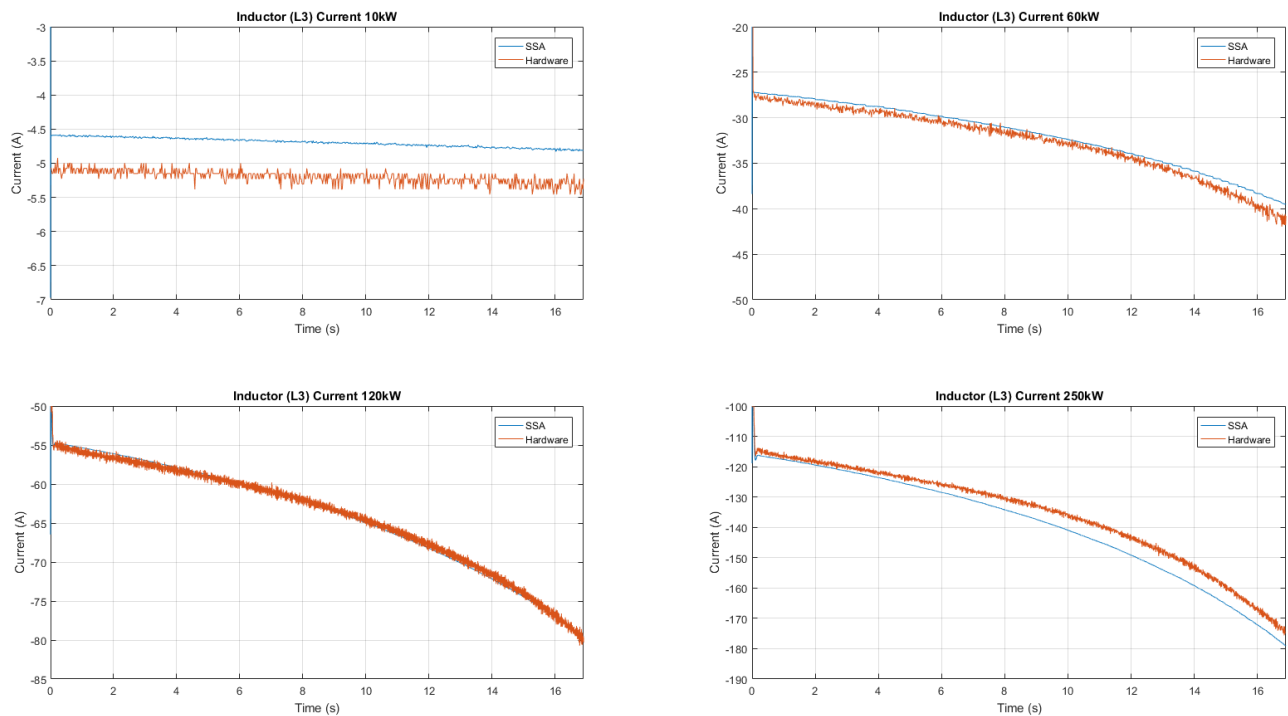
Figure 16 Current through the third inductor. (Blue) Results for the SSA model simulation. (Orange) Results for the hardware.
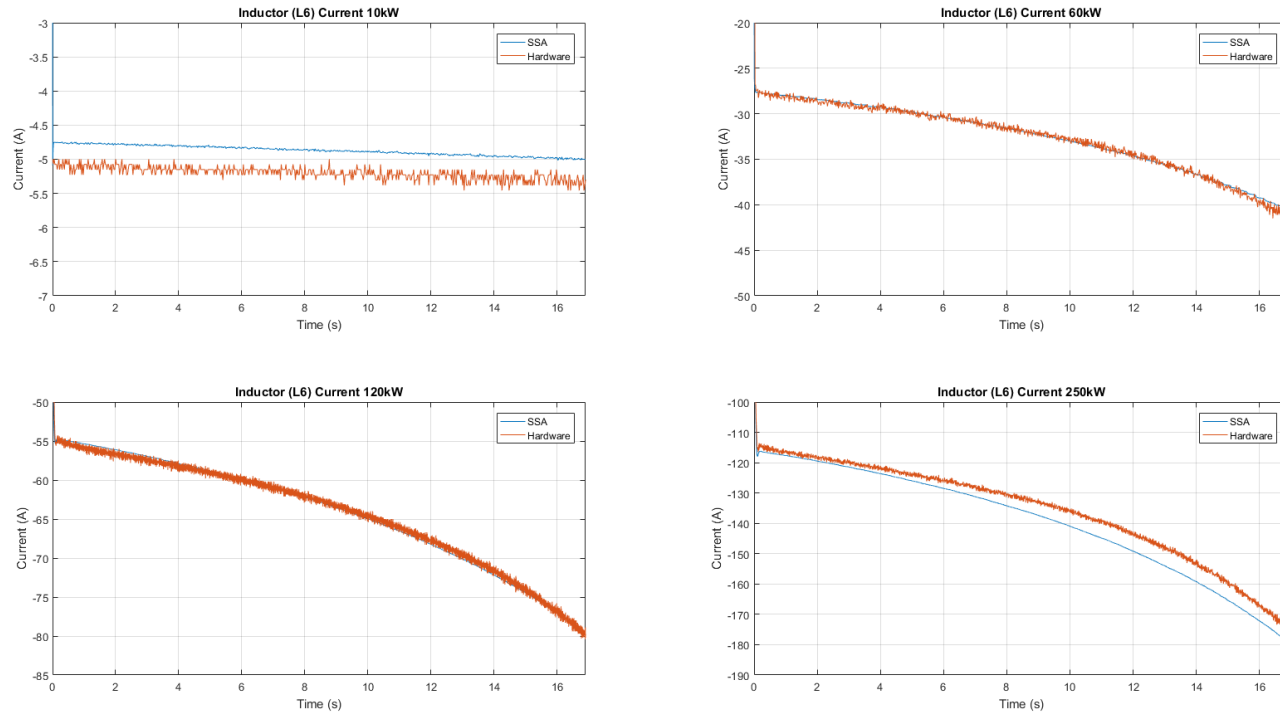
Figure 17 Current through the sixth inductor. (Blue) Results for the SSA model simulation. (Orange) Results for the hardware.

5.3.6 – Duty Cycle

Figure 18 Duty cycle for the third switch in the system for each trial. (Blue) Results for the SSA model simulation. (Orange) Results for the hardware.

Figure 19 Duty cycle for the sixth switch in the system for each trial. (Blue) Results for the SSA model simulation. (Orange) Results for the hardware.

5.4 – Overview of Simulation and Hardware Comparison
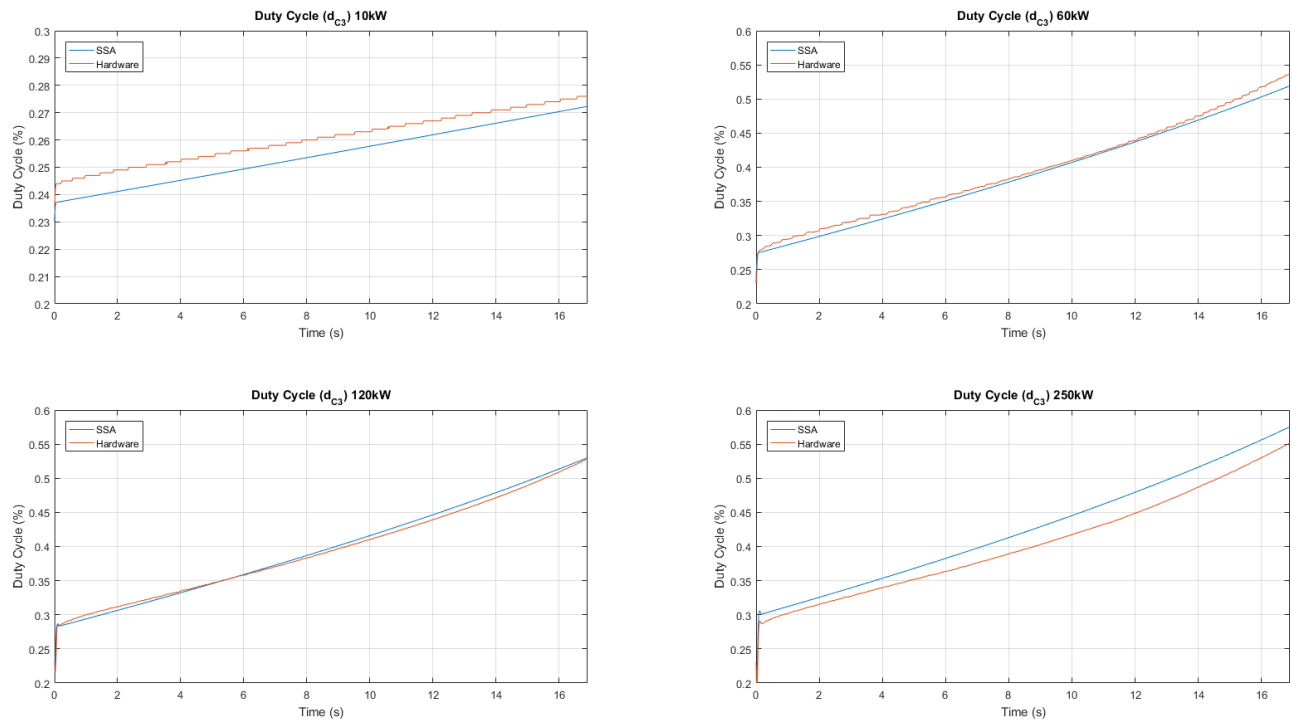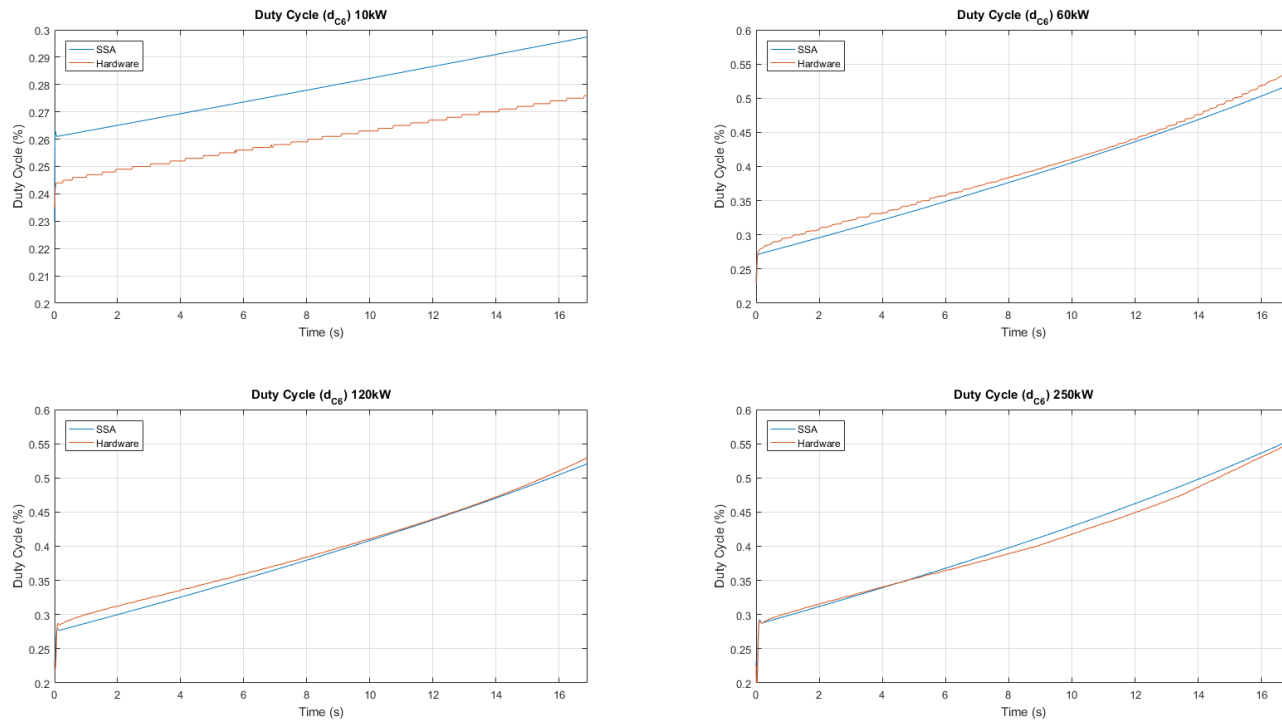
5.4.1 – Load Power, Current, and Voltage

The load power, current, and voltage for low (10kW), medium (60kW and 120kW), and high (250kW) outputs can be seen in Fig. 12–14. At every power output the simulation matches very closely with the hardware's experimental data for each parameter. There are negligible differences between the simulation and hardware thought to be caused by the fact that the simulation is based on a model for the average behavior of the system, and the experimental data fluctuates rapidly.

5.4.2 – Super Capacitor Voltage

The voltage for the supercapacitors (v_{LiC}) is shown in Fig. 15. At low (10kW) and medium (60kW and 120kW) power outputs, the SSA model was able to closely follow the general behavior of the hardware, with only small deviations. At the high (250kW) power output, there was a large deviation from 4–16 seconds.

5.4.3 – Inductor Currents

The current through two inductors (L_3 and L_6) are shown in Fig. 15 and Fig. 16, respectively. At the low (10kW) power output, there was a small, constant deviation between the SSA model and the hardware. For the medium (60kW and 120kW) outputs, the SSA model closely follows the hardware. At the high (250kW) output, there is a large deviation in the compared currents, beginning at 4 seconds.

5.4.4 – Duty Cycle

The duty cycle for two switches (d_{c3} and d_{c6}) are shown in Fig. 16 and Fig. 17, respectively. For the low (10kW) power output, there was a nearly constant difference between the duty cycles of the SSA model and the hardware. However, the constant error in d_{c3} was less than that for d_{c6}, which was reflected in the results for the inductor currents. The simulation also undershot the hardware's experimental data for d_{c3} and overshot it for d_{c6}. This is thought to be due to the fact that the duty cycle at this power level is low, where small errors would be more noticeable for the simulation.

For the medium (60kW and 120kW) outputs, the SSA model closely agrees with the experimental results of the hardware. At the high (250kW) power output, there was a deviation between the SSA model and hardware similar to that seen in the voltage of the supercapacitors at the same power output.

5.4.5 – Possible Reasons for Deviations at High (250kW) Output

The supercapacitor voltage, inductor currents, and duty cycles are all closely related as variables that belong to the input stage and come before the switches, and as such are more dependent on one another. The deviations at high (250kW) power output in these variables seems to be correlated and are thought to be caused by two sources. One is the compromise made involving the simplification of the final SSA model. Instead of considering all 64 possible states for the system, the SSA model approximates this with a combination of six simpler SSA models. The other is the fact that the SSA simulation's load resistance is low (1.23 – 1.27 Ω) and the current is high

(400–500A, see Fig. 13). At these extreme values, the simulation's parasitic

resistances could be more influential than in the hardware of the converter.

CHAPTER 6

CONCLUSION

6.1 – Overview

A state-space averaged model of hardware for a bidirectional DC-DC boost converter was developed. First, a general model of an ideal boost converter was derived. This was further developed to include a secondary inductor and parasitic resistances found in the hardware of the converter. Finally, a third model accounting for the non-ideal supercapacitor voltage source and the six inductors and switch pairs, each with their own duty cycle, was designed using the second model as a basis. This final model was implemented in Matlab/Simulink as a simulation and compared to experimental data recorded for the hardware.

For all power outputs, the simulation was able to match the hardware's experimental data for the load power, current, and voltage very closely. Minor deviations between the systems are believed to be due to the rapidly fluctuating nature of the hardware. This makes it difficult for an averaged model to agree exactly with the experimental data.

For variables that come before the switch: the supercapacitor voltage, inductor currents, and duty cycles, the simulation was found to be most accurate in the center range of the expected power outputs (60kW and 120kW) with the simulation agreeing very well with the experimental data of the hardware. At low power outputs (10kW), the simulation was able to capture the general behavior of the hardware, however there was a near constant difference in both the inductor currents and the duty cycles of the

system. For high power outputs (250kW), the simulation was initially able to follow the general behavior of the hardware converter, but was unable to match the hardware system near the end of the trial. There was an increasing difference between the simulation and hardware for the supercapacitors' voltage, inductor currents, and duty cycles.

Despite these discrepancies, the simulation was determined to be successfully accurate and will be used in optimizing the hardware converter.

6.2 – Future Work

This work will be used to predict dangerous levels of operation for the hardware, to optimize the control parameters in its control system, and to determine how to expand the system for a wider range of applications.

Motivation for the creation of the state-space averaged based simulation was the fact that the hardware converter had caught on fire twice during its design. This simulation will be used as a means to predict how the system could react without having to run a trial on the hardware that could damage it. This is necessary when components are exchanged, system parameters are altered, or when testing new power outputs.

The SSA model of the hardware will be used to optimize the control parameters of the control system. Previously, the control parameters for the converter were determined using an informed "guess and check" method due to the converters non-linearity. However, the SSA model offers the means to provide an approximate

linear description of a non-linear system (see Ch. 2.2.2). This allows for the use of control optimization techniques based on linear systems.

The hardware converter is designed with the ability to expand the system to meet a wider range of applications. This model will be used to ensure that when the converter is expanded, it will be done in an efficient manner. The SSA model and simulation easily allows for the addition of more inductors and switches, banks of supercapacitors, and changes to the control system. The model will allow for the prediction of how the converter will behave before having to build the full system with the actual hardware.

A.1 Implementation in Matlab/Simulink

A.1.1 Overview

The SSA model developed for the converter was implemented in Matlab/Simulink to simulate the real-world hardware. Implementing the model included designing subsystems for each of the state variables, as well as a system for replicating the control system used in the converter. Initializing key components such as the super capacitors' initial voltage and inductors' inductances was completed using the M-files listed in A.2.

A.1.2 Topology of Simulation

The hardware converter simulation implemented in Matlab/Simulink can be seen in Fig. 20.
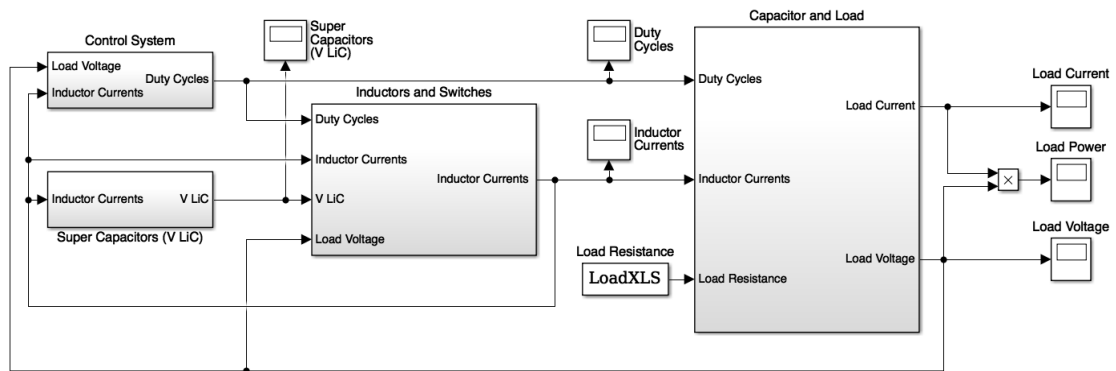

Figure 20 Overall topology of the SSA model simulation.

On the far left of the simulation is the "Supercapacitor" subsystem. This calculates the voltage level of the supercapacitors and inputs this into the subsystems for the inductors and switches. The inductors and switches subsystems calculate the

current for each inductor. These currents are sent to both the subsystem for the capacitor and load, and the controls subsystem.

The "Capacitor and Load" subsystem determines the voltage and current of the load. The voltage of the load is sent to the "Control System" subsystem. The current of the load is used with the voltage to determine the power output of the converter.

The "Control System" subsystem then calculates the appropriate duty cycle for each switch using the capacitor and load voltage, and the current through each inductor. These duty cycles are then sent to the "Inductors and Switches" subsystem and the "Capacitor and Load" subsystem.

The use of a "From Workspace" block can be seen for inputting the resistance of the load into the simulation. This block takes data from the Matlab workspace and feeds it directly into the simulation. In the hardware experimental tests, the load is simulated using a variable resistor. However, the resistance of the load has been known to fluctuate. To recreate the trials as accurately as possible, the resistance of the load was calculated using the data from the trials then saved in the Matlab workspace and loaded directly into Simulink during the simulation.

To record the values of each of these subsystems, "Scope" blocks are placed on their output. These "Scope" blocks saved the data to the Matlab workspace for use in analysis.

A.1.3 Systems in Simulation

Supercapacitor Subsystem
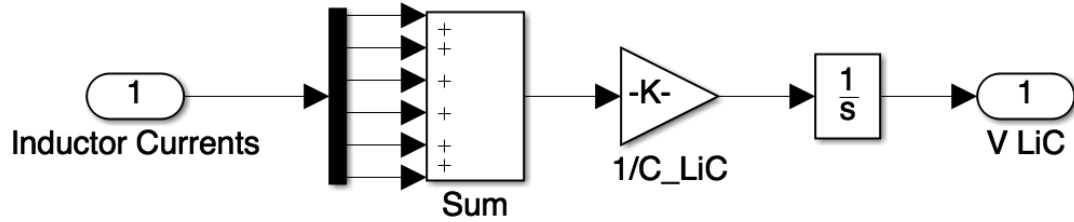
Figure 21 Diagram for the Super Capacitors subsystem.

The diagram of the subsystem for the calculating the voltage of the supercapacitors (V_{LiC}) is shown in Fig. 21. The voltage for the supercapacitors is calculated using the equation

$$v = \int -\frac{1}{C}\left(\sum_{i=1}^{6} i_{Li}\right) dt$$

The input "Inductor Currents" carries all six inductor currents. These are then summed, divided by the capacitance of the all the combined capacitors, then integrated using the $\frac{1}{s}$ block.

Inductors and Switches Subsystem

Figure 22 Diagram for the Inductors and Switches subsystem.

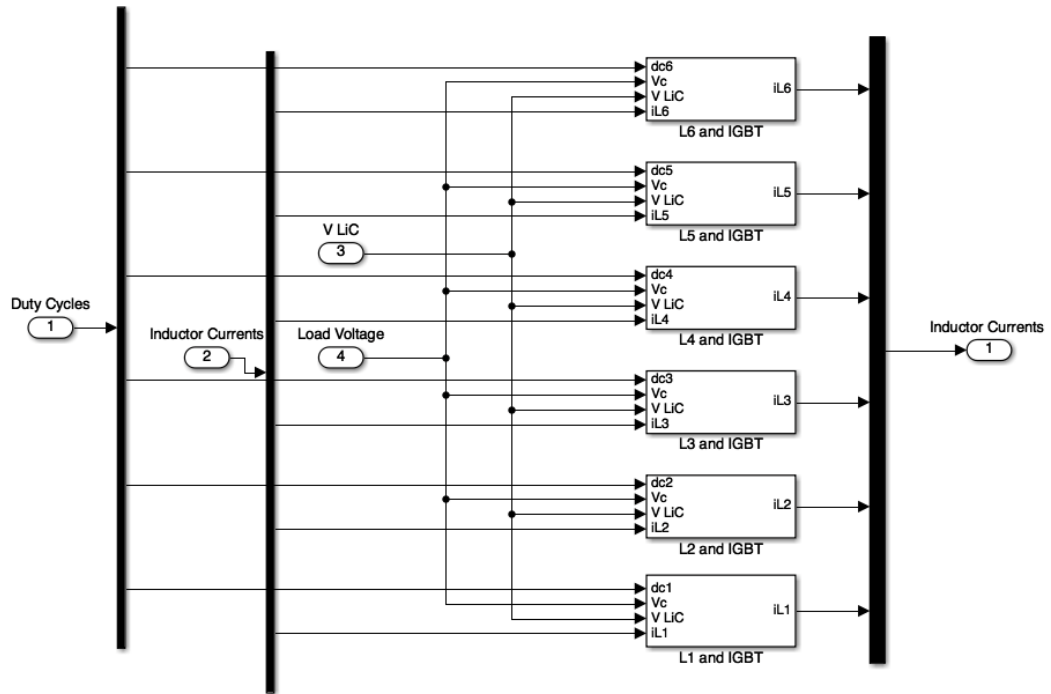In Fig. 22, the inputs are all six duty cycles, all six inductor currents, the voltage from the supercapacitors, and the load voltage. The duty cycles and inductor currents are separated into single values and sent to the appropriate inductor and switch pair.
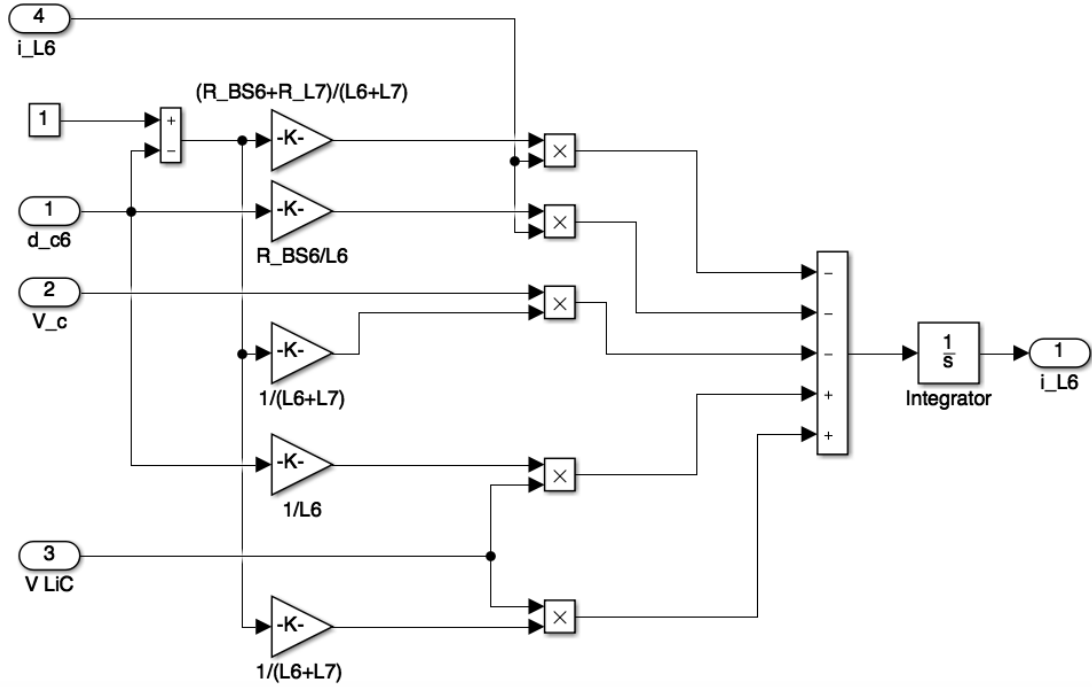
Figure 23 Diagram for the L6 and IGBT subsystem in the Inductors and Switches subsystem.

In Fig. 23, the calculation of a single inductor current (i_{L6}) is shown. This is calculated using the equation

$$i_{L6} = \int \left[\left(-\frac{R_{BS6}}{L_6} d_{c6} - \frac{(R_{BS6} + R_7)}{L_6 + L_7}(1 - d_{c6}) \right) i_{L6} - \left(\frac{1-d}{L_6 + L_7} \right) v_c \right.$$

$$\left. + \left(\frac{d_{c6}}{L_6} + \frac{(1 - d_{c6})}{L_6 + L_7} \right) v_{LiC} \right] dt$$

The inputs i_{L6}, d_{c6}, v_c, and v_{LiC} are multiplied by the appropriate values to create each term in the above equation. These terms are then summed and integrated to create the correct current for the sixth inductor.

The output from each inductor and switch pair is then combined into the single output named "Inductor Currents".

Capacitor and Load Subsystem
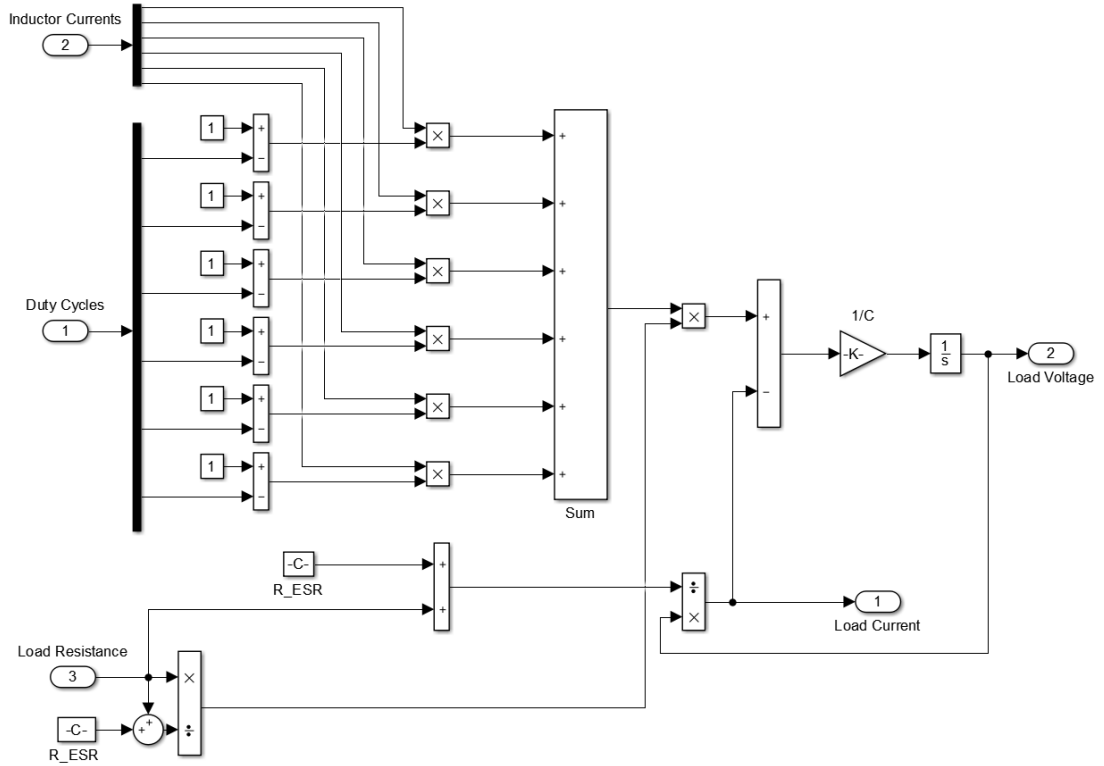
Figure 24 Diagram for the Capacitor and Load subsystem.

In Fig. 24, the inputs are all six duty cycles, all six inductor currents, and the load resistance. The equation for calculating the load voltage (v_c) is

$$v_c = \int \frac{1}{C} \left\{ \left(\frac{R_{Load}}{R_{Load} + R_{ESR} + R_7} \right) \sum_{i=1}^{6} [(1 - d_{ci})i_{Li}] - \left(\frac{1}{R_{Load} + R_{ESR}} \right) v_c \right\} dt$$

The duty cycles and inductor currents are separated into single values to form the sum then multiplied by the corresponding resistances. The v_c term is then subtracted from this sum and the value is divided by the capacitance of the capacitor in parallel with the load. This signal is then integrated and becomes the output "Load Voltage".

The output "Load Current" is calculated from the load voltage divided by the resistance of the load and the ESR of the capacitor.

Control Subsystem
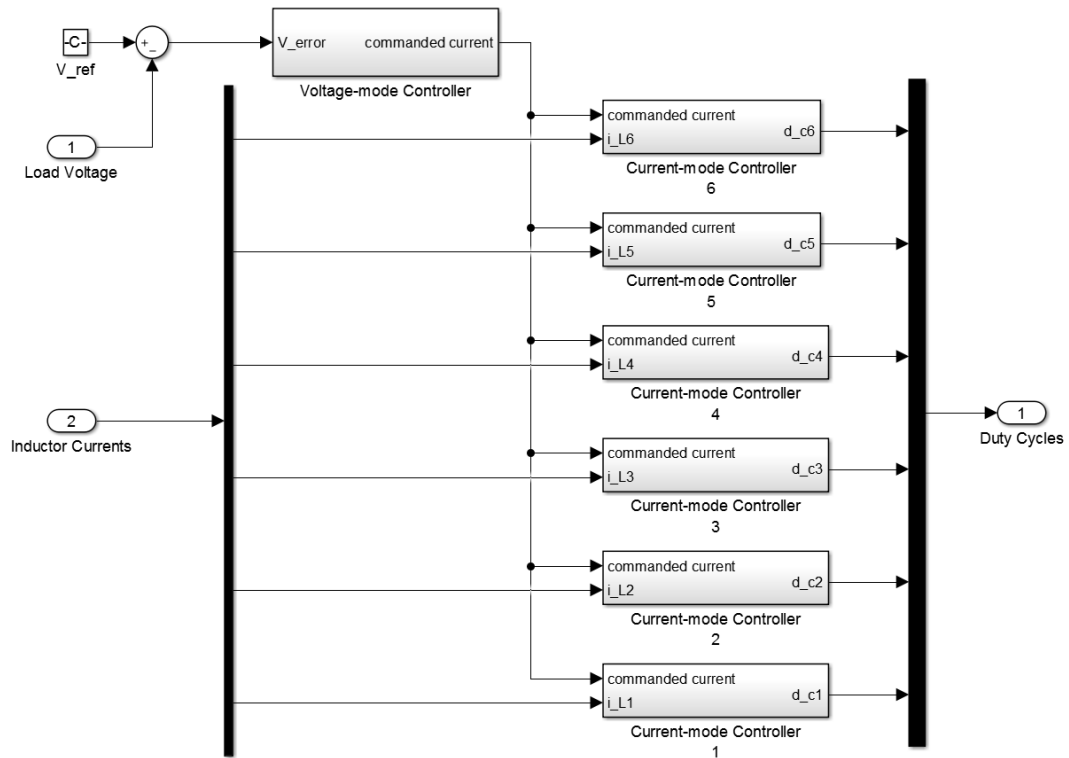
Figure 25 Diagram for the Control System subsystem.

In Fig. 25, a block diagram of the entire control system can be seen. The load voltage is compared to the reference voltage (V_{ref}) and the difference is sent to the voltage-mode controller. The voltage-mode controller determines the appropriate current for the inductors and this commanded current is sent to each current-mode controller where the appropriate duty cycle for each switch is calculated.

Figure 26 Diagram for the Voltage-mode Controller subsystem in the Control System subsystem.

Fig. 26 shows the system in the "Voltage-mode Controller" subsystem. The system is a direct implementation of a discrete time PI controller with output saturation using an anti-windup back-calculation method. The system follows the equation

$$I_{comm} = \left[k_{vp} + k_{vi} T_s \frac{1}{z-1} \right] V_{error} + k_{aw} \left(\frac{I_{sat} - I_{comm}}{z} \right)$$

Since there are six switches in the system, this commanded current is then divided by six to evenly distribute the current.
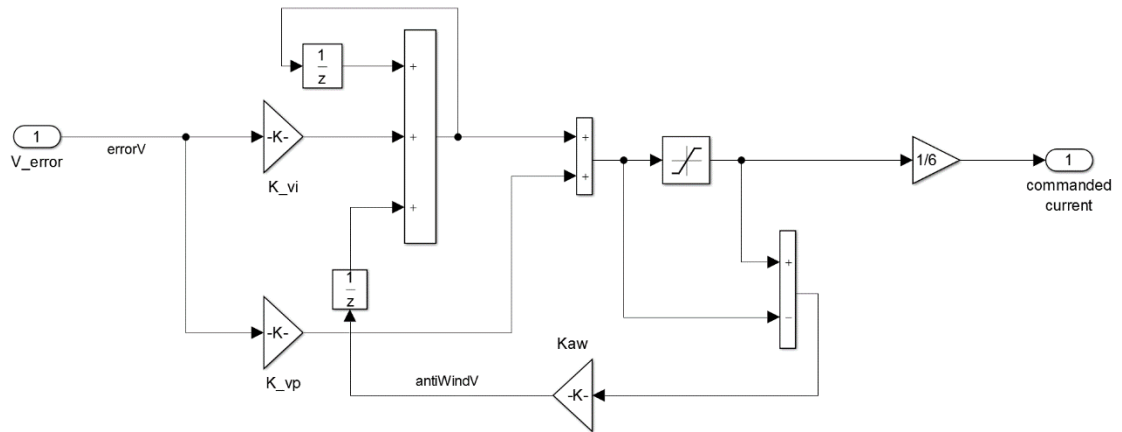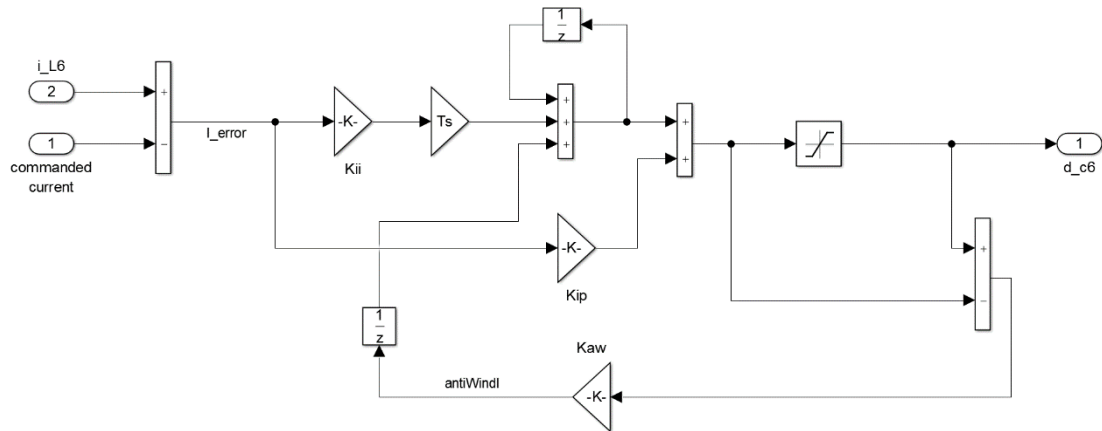
Figure 27 Diagram for the Current-Mode Controller 6 subsystem in the Control System subsystem.

Fig. 27 shows the system in the "Current-mode Controller 6" subsystem. The system is a direct implementation of a discrete time PI controller with output saturation using an anti-windup back-calculation method. First, the system finds the difference between the current in the inductor and the commanded current to find the current error (I_{error}), then the system follows the equation

$$d_{c6} = \left[k_{ip} + k_{ii} T_s \frac{1}{z-1} \right] I_{error} + k_{aw} \left(\frac{d_{c6\,sat} - d_{c6}}{z} \right)$$

A.2 M-Files for Simulations

A.2.1 – Values Constant for Each Simulation

```
%Overall system values
runT = 16.9;          %Run time of simulation
fs = 20e3;            %Switching frequency for system
Ts = 1/fs;            %Switching period for system
D1 = 0.23;            %Initial value for duty cycle


%Inductors in series with IGBTs
L1_I = 219.6e-6;      %Inductance for Inductor 1
L2_I = 213.0e-6;      %Inductance for Inductor 2
L3_I = 261.9e-6;      %Inductance for Inductor 3
L4_I = 237.4e-6;      %Inductance for Inductor 4
L5_I = 228.4e-6;      %Inductance for Inductor 5
L6_I = 218.1e-6;      %Inductance for Inductor 6
L1_R = 0.091;         %Resistance for Inductor 1
L2_R = 0.116;         %Resistance for Inductor 2
L3_R = 0.098;         %Resistance for Inductor 3
L4_R = 0.189;         %Resistance for Inductor 4
L5_R = 0.071;         %Resistance for Inductor 5
L6_R = 0.038;         %Resistance for Inductor 6


%Inductor in series with the load
L7_I = 1e-6;          %Inductance
L7_R = 0.0650;        %Resistance


%Capacitor || with the load values
C18_C = 1420e-6;      %Capacitance
C18_V = 520;          %Initial voltage
C18_R = 1.1e-3;       %Resistance



%Calculating the before switch resistance for each inductor and switch
R_BS = SC_R*1.2 + SCV_R;
R_BS6 = R_BS + L6_R;        %Resistance before switch 6
R_BS5 = R_BS + L5_R;        %Resistance before switch 5
R_BS4 = R_BS + L4_R;        %Resistance before switch 4
R_BS3 = R_BS + L3_R;        %Resistance before switch 3
R_BS2 = R_BS + L2_R;        %Resistance before switch 2
R_BS1 = R_BS + L1_R;        %Resistance before switch 1
```

A.2.1 – 10kW Trial M-file

```matlab
%Control System Values
Kvp = XX;          %Proportional Gain for voltage-mode controller
Kvi = XX;          %Integral Gain for voltage-mode controller
Kip = XX;          %Proportional Gain for current-mode controllers
Kii = XX;          %Integral Gain for current-mode controllers
V_ref = 520;       %Reference voltage
antiWindV = 0;     %Initial anti windup for voltage
Kaw = 1;           %Anti-windup coefficient


%Values for Super Capacitor Banks
numOfShelves = 1;                  %Number of shelves of caps: 1 shelf/60kW load
SC_C = 30.5556 * 0.85;             %Capacitance for 1 shelf
SC_C = numOfShelves * SC_C;        %Capacitance for all shelves
SC_V = 397;                        %Initial voltage
SC_R = 0.1 * 1.2;                  %Internal Resistance of 1 shelf
SC_R = 1./(numOfShelves./SC_R);    %Resistance for all shelves
SCV_R = 10e-6;                     %Connection Resistance


%Importing data for Load Resistance
    %Extracts data from Excel file used to record trial values
LoadXLS =
[xlsread('serial_sc10k.xls','serial_sc10k','A2:A801')-0.025
xlsread('serial_sc10k.xls','serial_sc10k','AB2:AB801')];
```

A.2.2 – 60kW Trial M-file

```matlab
%Control System Values
Kvp = XX;        %Proportional Gain for voltage-mode controller
Kvi = XX;        %Integral Gain for voltage-mode controller
Kip = XX;        %Proportional Gain for current-mode controllers
Kii = XX;        %Integral Gain for current-mode controllers
V_ref = 520;     %Reference voltage
antiWindV = 0;   %Initial anti windup for voltage
Kaw = 1;         %Anti-windup coefficient


%Values for Super Capacitor Banks
numOfShelves = 2;                %Number of shelves of caps: 1 shelf/60kW load
SC_C = 30.5556 * 0.85;           %Capacitance for 1 shelf
SC_C = numOfShelves * SC_C;      %Capacitance for all shelves
SC_V = 385;                      %Initial voltage
SC_R = 0.1 * 1.2;                %Internal Resistance of 1 shelf
SC_R = 1./(numOfShelves./SC_R);  %Resistance for all shelves
SCV_R = 10e-6;                   %Connection Resistance


%Importing data for Load Resistance
    %Extracts data from Excel file used to record trial values
LoadXLS =
[xlsread('serial_sc60k_gains3.4.xls','serial_60kw_gains3','A2:A1135')-0.015
xlsread('serial_sc60k_gains3.4.xls','serial_60kw_gains3','AA2:AA1135')];
```

A.2.3 – 120kW Trial M-file

```matlab
%Control System Values
Kvp = XX;         %Proportional Gain for voltage-mode controller
Kvi = XX;         %Integral Gain for voltage-mode controller
Kip = XX;         %Proportional Gain for current-mode controllers
Kii = XX;         %Integral Gain for current-mode controllers
V_ref = 520;       %Reference voltage
antiWindV = 0;  %Initial anti windup for voltage
Kaw = 1;          %Anti-windup coefficient


%Values for Super Capacitor Banks
numOfShelves = 3;                %Number of shelves of caps: 1 shelf/60kW load
SC_C = 30.5556 * 0.85;           %Capacitance for 1 shelf
SC_C = numOfShelves * SC_C;    %Capacitance for all shelves
SC_V = 385;                      %Initial voltage
SC_R = 0.1 * 1.2;                %Internal Resistance of 1 shelf
SC_R = 1./(numOfShelves./SC_R); %Resistance for all shelves
SCV_R = 10e-6;                   %Connection Resistance


%Importing data for Load Resistance
    %Extracts data from Excel file used to record trial values
LoadXLS =
[xlsread('120kw_new_gains.xlsx','120kw_new_gains','A2:A4251')-0.004
xlsread('120kw_new_gains.xlsx','120kw_new_gains','AA2:AA4251')];
```

A.2.4 – 250kW Trial M-file

```matlab
%Control System Values
Kvp = XX;         %Proportional Gain for voltage-mode controller
Kvi = XX;         %Integral Gain for voltage-mode controller
Kip = XX;         %Proportional Gain for current-mode controllers
Kii = XX;         %Integral Gain for current-mode controllers
V_ref = 520;      %Reference voltage
antiWindV = 0;    %Initial anti windup for voltage
Kaw = 1;          %Anti-windup coefficient


%Values for Super Capacitor Banks
numOfShelves = 4;                     %Number of shelves of caps: 1 shelf/60kW load
SC_C = 30.5556 * 0.85;                %Capacitance for 1 shelf
SC_C = numOfShelves * SC_C;           %Capacitance for all shelves
SC_V = 385;                           %Initial voltage
SC_R = 0.1 * 1.2;                     %Internal Resistance of 1 shelf
SC_R = 1./(numOfShelves./SC_R);       %Resistance for all shelves
SCV_R = 10e-6;                        %Connection Resistance


%Importing data for Load Resistance
     %Extracts data from Excel file used to record trial values
LoadXLS =
[xlsread('250kw_4p_newcapsgains.xls','250kw_4p_newcapsgains','A2:A2255')-0.0196
xlsread('250kw_4p_newcapsgains.xls','250kw_4p_newcapsgains','AF2:AF2255')];
```

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