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Field-programmable gate array-controlled sweep velocity-locked laser pulse generator

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Abstract. This manuscript reports a FPGA-controlled sweep velocity-locked laser pulse generator (SV-LLPG) design based on an all-digital phase-locked loop (ADPLL). A distributed feedback (DFB) laser with modulated injection current was used as a swept-frequency laser source. An open loop pre-distortion modulation waveform was calibrated using a feedback iteration method to initially improve frequency sweep linearity. An ADPLL control system was then implemented using a field programmed gate array (FPGA) to lock the output of a Mach–Zehnder interferometer that was directly proportional to laser sweep velocity to an on-board system clock. Using this system, linearly chirped laser pulses with a sweep bandwidth of 111.16 GHz were demonstrated. Further testing evaluating the sensing utility of the system was conducted. In this test, the SV-LLPG served as the swept laser source of an optical frequency domain reflectometry (OFDR) system was used to interrogate a sub-terahertz range fiber structure (sub-THz-FS) array. A static strain test was then conducted and linear sensor results were observed.

Keywords: interferometry, fiber optics, laser applications.

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1 Introduction

Frequency modulated continuous wave (FMCW) reflectometry or optical frequency domain reflectometry (OFDR) (1-3), is a well-established frequency domain measurement method for optical component characterization and optical fiber distributed sensing. This technique allows distance domain information to be obtained from frequency domain intensity data via a Fourier transform. A key component of this FMCW reflectometry system is a swept-frequency laser source. A variety of laser sources have been investigated for this purpose, including temperature and piezo-electrically tuned Nd: YAG ring lasers (4, 5), external cavity lasers (ECLs) (6-10), piezo-electrically tuned fiber grating lasers (11), and chirped distributed feedback (DFB) lasers (12).

Among these sources, the chirped DFB laser represents a particularly promising candidate for narrow-bandwidth interrogation applications. The output frequency of DFB lasers can be controlled using injection current modulation without the need for any moving mechanical components, resulting in a fast repetition rate over a sweeping bandwidth of ~ 100 GHz. Other beneficial features of chirped DFB lasers include single longitudinal mode output, good laser coherence length (\sim km), and low cost. However, there are several drawbacks limiting chirped DFB lasers as elements of FMCW/OFDR systems. Chief among these is a non-linear relationship between input current and output frequency, leading to non-linear optical sweep speeds. To compensate this non-linearity, a pre-distortion waveform can be generated based on a feedback iteration method (13). However, this method only fractionally enhances the linearity of the resulting optical sweep speed. An auxiliary clock or ‘k-clock’ with a fixed optical delay can also be applied to resample the data and correct for non-linear sweep speeds (13). However, this sampling clock method increases both system sampling and signal processing complexity.

A closed loop control system based on an optical phase-locked loop (OPLL) that modifies laser output frequency in real-time offers an alternative approach to precisely controlling optical sweep speed (14, 15). Recently, a digital-controlled chirped pulse laser based on a digital phase-locked loop (DPLL) design was reported based on modular electronic design (16). A digital phase comparator (XOR gate) was utilized to extract phase errors between the output of a Mach-Zehnder interferometer, which converted laser sweep speed to a radio-frequency signal, and a reference oscillator. The system generated a highly linear frequency sweep, and its utility as a source for high spatial resolution fiber sensing applications was demonstrated. However, while this system successfully demonstrated the concept, there remain engineering challenges, stemming from the fact that analog systems are susceptible to noise and DC drifts in comparison to similar digital

systems (17, 18). More importantly, modular design results in relatively high power consumption, large size and weight of the final product.

This manuscript reports an alternative design for a sweep velocity-locked laser pulse generator (SV-LLPG) using an all-digital phase-lock loop (ADPLL), which has the potential to surmount several of the previous engineering challenges facing modular DPLL design. The ADPLL is constructed such that all components, including the phase comparator, loop controller, and reference frequency synthesizer, are digitally generated using logic gates and integrated in an IC chip. This design was then implemented using a field-programmable gate array (FPGA) in which all digital components were synchronized using the same on-chip clock to minimize phase noise. The FPGA chip used in this design is from Xilinx Zynq 7000 series, and the DAC is a Texas Instruments DAC121S101 with 12-bit resolution and a sampling rate of 1 MSa/s. Using this approach, a sweeping bandwidth of 111.16 GHz over 9 ms has been demonstrated. A highly consistent sweep velocity of 12.35 GHz/ms is maintained within each chirped pulse. The standard deviation of the starting frequency was measured to be 106.7 MHz, corresponding to a strain sensing instability of $0.79 \mu\epsilon$. In order to evaluate the potential of the ADPLL-based SV-LLPG as an element of an OFDR system, the system was used to interrogate a sub-THz-FS array. Highly linear results and a sensitivity of $-0.1346 \text{ GHz}/\mu\epsilon$ were observed, which agrees well with previously reported sensing results obtained using an ECL (6, 7).

2 Operational Mechanism

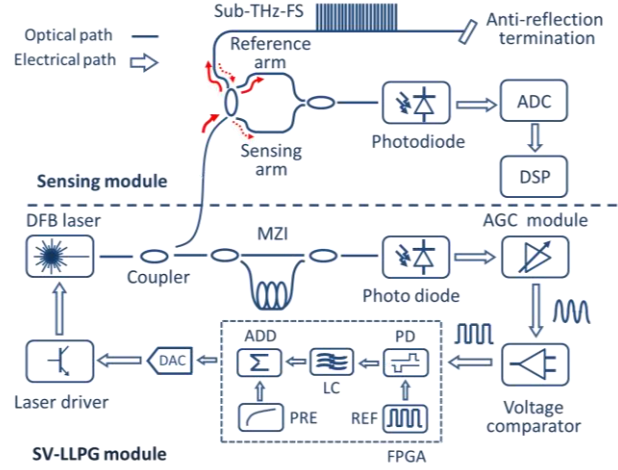


Fig.1 Schematic of proposed all-digital OPLL system with sensing module and control module (MZI: Mach-Zehnder interferometer; FPGA: field-programmable logic array; DAC: digital-to-analog converter; ADD: adder; PRE: pre-distortion curve; LC: loop controller; REF: reference frequency clock; PD: type-II phase detector; ADC: analog-to-digital converter; DSP: digital signal processing unit).

A schematic of the described interrogation system is shown in Fig. 1. In the SV-LLPG module, a DFB laser is employed as the frequency sweep source, which is injection current-modulated using a time-varying voltage via a laser control circuit. An isolator is placed at the laser output to eliminate reflection. Using a 90/10 coupler, 10% of the output power is directed in to the MZI and 90% of the power into the sensing module to interrogate the sub-THz-FS array. The MZI is constructed with two 3-dB couplers with a constant delay, τ_d , of 11.334 ns. Under the assumption that the DFB laser is operated at a constant sweep velocity, the AC-coupled current output $i(t)$ at the photo diode after the MZI as a function of time can be expressed as:

$$i(t) = \frac{A(t)^2}{8} \eta \cos[2\pi(f_0 + vt)\tau_d] \quad (1)$$

where $A(t)$ is the electrical-field amplitude directed into the MZI as a function of time, η is the responsivity of the photo diode, f_0 is the initial frequency of the DFB laser during sweeping, v is the optical sweep velocity, and t is the time. A beat frequency in the radio frequency (RF) range less than 250 kHz, which is linearly proportional to laser sweep velocity, is generated through this fixed delay MZI. Due to the current injection modulation, the intensity of the DFB laser output

varies as a function of time. To account for this effect, an automatic gain control (AGC) transimpedance amplifier is used to adjust the amplitude of AC-coupled photodiode output signal. This photodiode has a bandwidth of 1MHz. A high-speed voltage comparator with a bandwidth of 50 MHz is used to convert the analog beat signals into digital signals, which is sent into a digital input port of a FPGA evaluation board with a 100 MHz system clock. In order to improve the initial laser sweep linearity before phase locking, a pre-distortion voltage waveform is pre-calibrated using a feedback iteration method (13), resulting in an output frequency sweep velocity at about 12.5 GHz/ms. This open loop pre-distortion voltage waveform is then stored within the FPGA memory. A type-II phase comparator, constructed with two D flip-flops and an AND gate (19), is used to extract the phase difference between the input digital signal and the on-board reference frequency clock f_R at 140 kHz. The resulting phase error signals are then fed into a loop controller constructed using an integrator to further modify the pre-distortion current modulation waveform. The digital output of the FGPA is converted to an analog signal using a digital-to-analog converter (DAC) module with a refresh cycle of 1 μ s and sent to the laser driver circuit.

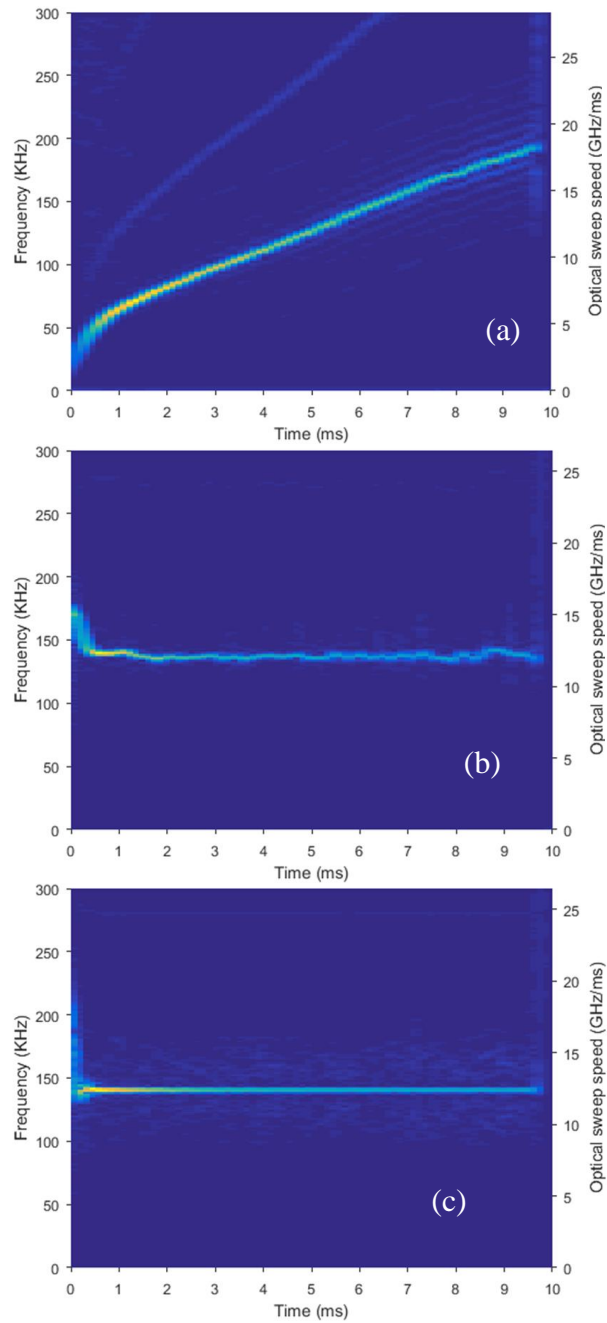


Fig.2 Measured frequency spectrum of AGC output within a chirped laser pulse: (a) free running with ramp input; (b) free running with calibrated pre-distortion input; (c) sweep velocity locked.

Spectrograms of the AGC output during a chirped laser pulse under the free-running open loop case (when the phase errors are not fed into the loop controller) with an unmodified ramp input and under the pre-calibrated modulation waveform case are shown in Fig. 2 (a) and (b). Sweep

linearity is substantially improved using the pre-distortion curve compared with the initial ramp waveform. After closing the control loop (i.e. when the phase errors are fed into the loop controller), the laser sweep velocity is locked during each chirped laser pulse. When locked, the AGC output signal is in phase with the digital reference clock and the locked optical frequency sweep velocity ν can be expressed as:

$$\nu = \frac{f_R}{\tau_d}. \quad (2)$$

Given the fixed MZI delay length τ_d and the digital reference clock frequency f_R , the locked sweep velocity is calculated to be 12.35 GHz/ms. Fig. 2 (c) shows the AGC output within a chirped pulsed under the locked condition. The total locking period within the chirped pulse is approximately 9 ms, leading to an optical sweeping bandwidth of 111.16 GHz. Fig. 3 (a) shows the Fourier transform of the AGC output over the span of 9 ms under the locked condition; over that span, a signal-to-noise ratio (SNR) above 35 dB was achieved. During testing, a resting period of 10 ms followed each 10 ms sweep in order discharge the capacitor within the laser driver circuit, resulting

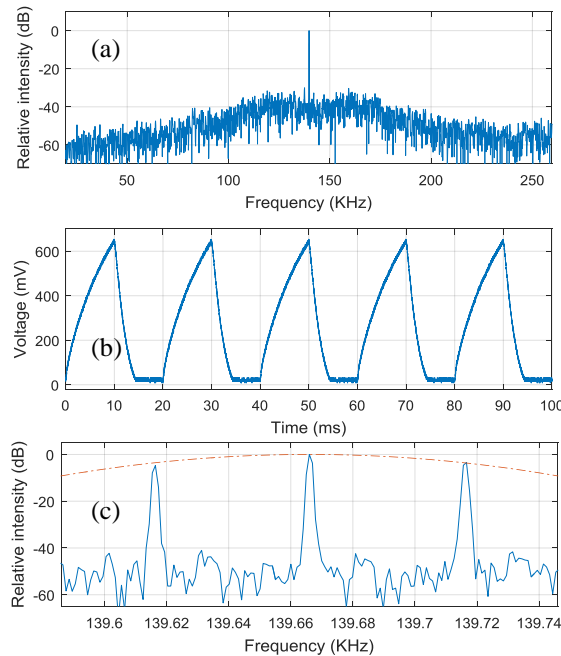


Fig.3 (a) Fourier transform of the AGC output over the locked span of 9 ms; (b) output of the laser pulse generator with 5 complete cycles; (c) a Gaussian curve fit applied to measure the FWHM of the Fourier transform of a chirped pulse train over 1 second.

in a total period of 20 ms for each complete pulse cycle and a repetition rate of 50 Hz. The output of the chirped laser pulse generator for 5 complete cycles at the photodetector is plotted in Fig. 3 (b). To determine the noise of the system, 1 second of data with 50 chirped laser pulses was recorded. The Fourier transform of this data is plotted in Fig. 3 (c). A center frequency of 139.667 kHz was found. A 50 Hz frequency period was observed due to the repetition rate described above. The full width at half maximum (FWHM) of the peak envelope using a Gaussian curve fit was measured to be 90 Hz.

Along the sensing module, a homodyne interferometry structure is constructed using two 2×2 3-dB couplers as shown in Fig. 1. The input light is split into two paths via the first coupler, with one serving as reference arm and the other path directed into the sensing arm, which includes a sub-THz-FS array. The sensing arm is terminated using an anti-reflection cut. The reflected light from the sub-THz-FS is then combined with light from reference arm via the second coupler. A photodetector and a single channel AC-coupled 8-bit analog-to-digital converter (ADC) is used to record the resulting data. The sampling rate of the ADC is set to 8 MSa/s with a match anti-aliasing filter. The digitized raw data is then fed into a DSP module.

3 Experimental Results

In order to investigate the sensing capability of the described SV-LLPG system, a 20-pt periodic weak reflection sub-THz-FS array with a 1 mm pitch length was fabricated along a single mode fiber (SMF-28, Corning, Inc.) using a Ti: Sapphire femtosecond laser micromachining system (Coherent, Inc.) (6, 7, 20, 21). During interrogation and signal processing, this sub-THz-FS array was considered to be 9 cascaded sub-THz- grating sensor units using a 4-mm wide moving Butterworth bandpass filter with a step size of 2-mm. Each sensor unit contains 4 reflection peaks. This signal processing method has been systematically investigated in the previous publications

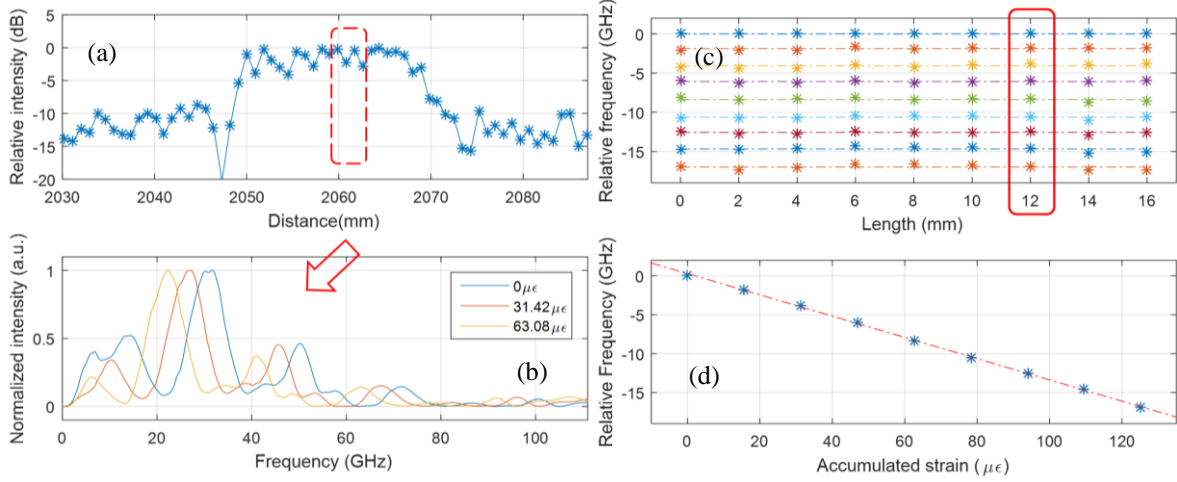


Fig. 4 Static strain test: (a) time domain reflections of DUT; (b) interferograms of the sensor unit between 1779 mm and 1783 mm with varied strain applied; (c) strain test results for all 9 sensor units; (d) strain test results of for 7th sensor unit.

(7, 22). A self-mixing method and a low pass filter is applied to extract the resulting interferograms. Changes in strain along the optical fiber result in optical path length (OPL) changes between the weak reflectors, which generate a phase-shift in the interferograms that are used to measure strain changes along the sensor probe.

To evaluate the strain sensing capability of the system, a series of static strain tests were conducted. One end of the fiber under test (FUT) was secured to an optical bench while the other end was left free to hang. Weights were sequentially added to the free end of the fiber at 1.33 g intervals; in total 10.64 g of weights were added to the free end of the FUT, resulting in a strain change of 125.23 $\mu\epsilon$. The SV-LLPG system was set using the parameters described above, resulting in a total sweeping bandwidth of 111.16 GHz. The resulting distance domain signals, calculated using a Fourier transform and in which the sensor structures can be identified between 2047 mm and 2067 mm, are plotted in Fig.4 (a). Due to the limited interrogation bandwidth, the individual reflection peaks of the sub-THz-FS array elements cannot be resolved. The measured frequency domain interferograms of the 7th sensor unit between 2059 mm and 2063 mm are plotted in Fig. 4 (b). The strain test results for all 9 sensor units are plotted in Fig. 4 (c), and the results of the 7th sensor unit specifically are plotted in Fig. 4 (d). Linear results were observed for all sensor

units, with the least linear having a R^2 value of 0.9986. The mean strain sensitivity across all sensing elements was calculated to be $-0.1346 \text{ GHz}/\mu\epsilon$ with a standard deviation of $0.0026 \mu\epsilon$. The start sweep frequency was evaluated by measuring the starting frequency of the entire system over 1000 captures, and the standard deviation of start frequency was 106.7 MHz.

4 Conclusions

To conclude, this manuscript reports a FPGA-controlled sweep velocity-locked laser pulse generator (SV-LLPG) design. A DFB laser is employed as the sweep source and an ADPLL control system is used to lock the laser sweep velocity to an on-board reference clock. Highly linear chirped laser pulses with a bandwidth of 111.16 GHz were demonstrated. A sweep velocity of 12.35 GHz/ms was achieved for 9 ms within each chirped pulse at a 50 Hz pulse repetition rate. To investigate system sensing utility, the SV-LLPG prototype was used as an element of an OFDR system to interrogate a sub-THz-FS array. A static strain test was conducted and highly linear results were observed.

The proposed device holds the promise to deliver a low size, weight and power (SWaP) and affordable interrogator for distributed fiber sensing applications. In addition, the FPGA based design makes it easier to be integrated and adopted for various applications in the future.

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Tao Wei received his B.S. degree in mechanical engineering from Nanjing Technology University in Nanjing, China in 2006, and his M.S. and Ph.D. degrees in electrical engineering from Missouri University of Science and Technology in Rolla, MO, USA in 2008 and 2011, respectively. He is currently an Assistant Professor of Electrical Engineering at the University of Rhode Island in

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Caption List

Fig. 1 Schematic of proposed all-digital OPLL system with sensing modulate and control module (MZI: Mach-Zehnder interferometer; FPGA: field-programmable logic array; DAC: digital-to-analog converter; ADD: adder; PRE: pre-distortion curve; LC: loop controller; REF: reference frequency clock; PD: type-II phase detector; ADC: analog-to-digital converter; DSP: digital signal processing unit).

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